Cascade SiT9514x GUI Release Notes

Contents

1. Version 1.0015 [27-Oct-2018]

1. Fixed: Debug of SE type complimentary checker (warning display enabled).
2. Fixed: Debug of output driver type related warnings (warning display enabled).
3. Fixed: Update the default I2C address of SiT95147 to 0x6D.
4. Fixed: Debugged dividers calculated for long trailing fraction input. Update of default file for the backend to ensure more efficient divider calculation. This was an issue in the previous versions for long trailing fractions that needed more than 31 bits for representation.
5. Fixed: Debug loading of doubler enablement from input files.
6. Fixed: Debug of embedded MEMS Clock Loss status in Realtime window. In Realtime status window XO Clock Loss status was not reflecting correctly.

2. Version 1.0016 [17-Nov-2018]

1. Fixed: The GUI had an issue with bandwidth and parameter allocation for non-continuous PLL mapping due to a misinterpretation of the array allocation in Python by the software engineer. If the input was all four PLLs (A, B, C, D) or first 2 PLLs (A, B) or 3 PLLs (A, B, C) it was not an issue. When the PLL was discontinuous it assumed that the parameters were for disabled PLLs which as a feature are ignored during writing. We have corrected the mapping and the updated executable should not have this error. For example: if you set two PLLs (A, D), the PLLD will not be mapped correctly when you set the Fast bandwidth and Normal bandwidth in the GUI for Version 1.015. It will use its default Fast and Normal loop bandwidth for customer's application requirement. This is corrected in Version 1.0015A

3. Version 1.0017 [24-Nov-2018]

1. Fixed: Frequency on the fly feature is implemented as part of the GUI. This involves the creation of 4*N static profiles for the case of N frequencies requested from the PLL.
2. Fixed: Au5310 test versions are dropped and only SiT95147 and SiT95141/5 options are provided.

4. Version 1.0018 [7-Dec-2018]

1. Fixed: Frequency on the fly feature is implemented such that it is usable for multiple outputs from a PLL. All these outputs from a PLL are required to be at the same output frequency.

5. Version 1.0019 [25-Dec-2018]

1. Fixed: Frequency on the fly feature is implemented such that it is usable in conjunction with the dynamic embedded code that is delivered separately as a Python code set.

6. Version 1.0020 [7-Jan-2019]

1. Fixed: SPI is usable now from the GUI. Can generate a SPI based register write sequence as well as write SPI to the Aura EVK after suitable board modifications.
2. Fixed: The Frequency change on the fly can now be used for multiple outputs from the same PLL that are integer related to each other. In V1.0018 the multiple output on-the-fly implementation needed all the outputs from a PLL to be at the same frequency.
3. Wake up time related enhancement. Fast Bandwidth (instead of Normal Bandwidth) settling time is now used to enable the output clock during power-up to reduce the wake-up time. Updates are in registers 0x2A in PLL page.

7. Version 1.0021 [25-Jan-2019]

1. Changed the dynamic files generated by the GUI to be compatible with the dynamic C code for on-the-fly applications. These are *.json files.
2. Capability to create an I2C file to burn the fuse for any profile from the GUI itself.

8. Version 1.0022 [8-Mar-2019]

1. Added the SiT95148 product variant as a usable option in the GUI.
2. Default resolution for ppm measurements for frequency ramp is improved for finer frequency ramp performance.
3. Dynamic on the fly performance check is now possible from the GUI itself
    a. Same algorithm as the dynamic on the fly C code is implemented in the background now by the GUI. This is a very useful tool for testing the performance of the dynamic algorithm for any profile using the GUI and the EVK itself
4. New header file is created for the dynamic OTF operation from the C code
    a. This optimizes the storage for the use of the C code in the system if the state needs to be saved in case of a system reset
5. Adjacent SE and DE outputs spur coupling warning is removed if the outputs are from the same PLL.
6. There was an issue with the “load NVM” function for some cases which is now resolved. This is a feature that can be used for loading an i2c or spi file to directly write to the part from the GUI itself.

9. Version 1.0023 [9-May-2019]

1. Added doubler enabled as default for LFF.
2. Warning on crystal LFF used < 80 MHz.

3. Low Wander mode is usable that can be used for combining the wander of an OCXO/TCXO with the jitter of the embedded MEMS for low wander holdover applications. This should have no impact on users that do not use this mode.

10. Version 1.0024 [30-May-2019]

1. Added an indicator in the RealTime window for actual exact PLL BW that is programmed.
    a. Made small improvement in accuracy of BW by modifying an internal parameter.
2. Enhanced the input divider capability to find multi input solutions using fractional input dividers for very largely spaced input frequencies also.

11. Version 1.0025 [23-Jul-2019]

1. Changed the embedded MEMS Loss Alarm monitoring mode.
    a. This is a more robust XO loss detection alarm.
2. Added a chip reset at the beginning of every profile in the I2C / SPI nvm profile file generated from the GUI.
3. Added additional modes for robustness to transient performance behavior in the case of sporadic input clocks.

12. Version 1.0026rc8 [7-Sep-2019]

1. Address for I2C based chip reset release now incorporates the state of the pin based I2C address.
2. Added a current consumption calculator in the Real Time window for current consumption estimate from each supply for any given profile.
3. For the SiT95141/5 parts where all the PLLs share the same input clock priority, PLLs can be selectively chosen as “Free Run”.
4. The register sequence and config files generated from the GUI now have the GUI version mentioned as a line at the top of the file.

13. Version 1.0027.5 [6-Dec-2019]

1. Direct provision to burn efuse from the GUI itself and feature to verify the efuse contents on a fuse locked part.
2. GCD (Greatest Common Divisor) based calculation for the internal input frequencies is improved for the case of frequency ramp being enabled. Earlier the GCD was calculated for all input frequencies for the case of frequency ramp being enabled for any PLL. Now this is done specifically for the inputs to the PLL that is doing the frequency ramp.

3. Higher robustness options in software wake up sequence for the case of input clock coming in later than wake up for the case of input dividers.

4. Speed up for frequency ramp measurement is done for the case of low input frequencies.

14. Version 1.0028 [2-Feb-2020]

1. There was an issue in the previous GUI release (v1.27.5) with respect to Item 3 in the change list for GUI version 1.0027.05. This errata item will impact the clock switch operation for all the profiles which has Frequency Ramp Enabled in the profile when IN0 is selected as Input and an input divider is used. It doesn't impact the profiles where IN0 is not selected as an Input and the Frequency Ramp is enabled. This is resolved in version 1.0028. This will need an upgrade to v1.0028 for all such profiles that have IN0 enabled and Frequency Drift is enabled only for cases where the profile is generated using GUI version 1.27.5.

2. For DCO Mode on the outer PLL, some additions are made for faster and more robust transient performance improvement.

3. Phase sync mode is added in the GUI. This feature means that post power up, the outputs from various PLLs will maintain the same relative phase difference even in Holdover when input clocks are lost. This feature is provided by a cascade PLL arrangement where PLLA determines the PLL dynamics and PLL B, C, D (one or more of B, C, D) can be used as slave PLLs that work on an embedded MEMS reference that is derived from the outputs of PLLA. Hence for slave PLLs in the Phase Sync feature the PLL parameters are disabled for user entry since the slave PLLs respond to the dynamical behavior of the PLLA master. Using this feature is recommended only for cases where the output phases are expected to stay in sync across different PLLs even with loss of input clock. For all other cases using this is not recommended since there is a small noise penalty for using two PLLs in cascade.

4. A warning message is added when loading an efuse write capable nvm file to alert the user that the efuse will be burned on the part.

5. Higher level of information regarding output VDD and output standard is displayed for each output on the Bird's Eye View and miscellaneous readability enhancements are done.

15. Version 1.0029.1 [13-Apr-2020]

1. SiT9514x variants have been split to SiT95145 and SiT95147 accordingly to take care of the VDDIO selection based on the mask revision.

This selection of VDDIO has been implemented in the V1.29 for SiT95141x production parts based on the table:

Table 1:

Variant	Mask Revision	Default VDDIO Power Up	VDDIO=VDD	VDDIO=VDDIN
SiT95141x	Rev C1	VDDIN	0x23[7]=1, Page0	0x23[7]=0, Page0

SiT95141x	Rev C1	VDD	0x23[7]=0, Page0	0x23[7]=1, Page0

16. Version 1.0030.4 [14-Sep-2020]

1. The VDDIO selection has been modified to take care of SiT9514x variants based on the table below:

Table 2:

Variant	Default VDDIO Power Up	VDDIO Selection	VDDIO Support
SiT95145	VDD	VDD{0x23[7] =0, Page0}	1.8 V
SiT95145	VDDIN	VDD{0x23[7] =1, Page0}	3.3 V
SiT95147	VDD	VDD{0x23[7] =0, Page0}	1.8 V
SiT95147	VDDIN	VDD{0x23[7] =1, Page0}	3.3 V

2. The PLL Input Priority Order is disabled when the Input Selection is set to Manual for the SiT95141/5 and SiT95147/8 variants.

3. FLEXIO functionality is enhanced to bring out all possible Input and PLL status/notify status on the available FLEXIO's for SiT95141/5 and SiT95147 variants based on the Application Note AN20008 (FlexIO Mapping).

4. IN3 clock selection for any of the PLL's is disabled when IN3 Sync and ZDB feature is used.

5. Updates done to the OTF feature to incorporate the support for very low frequency clocks.

6. The I2C spike suppression circuitry is enabled for the I2C Interface as per the table below right at release of reset of the chip.

Table 3:

Interface	HS_EN	Spike Suppression Circuit	0xE2
SPI	1	Unused	0x00
I2C	0	Used	0x01

17. Version 1.0032.7 [19-Sep-2022]

1. Fixed: Fix loading invalid FlexIO clkmon_def legacy files.
2. Make free running frame widgets editable when LWM and phase sync mode are enabled.
3. Fixed: In OTF dump the file gets overwritten when it has same name. This happens when the floating numbers are ignored. So, added as many digits needed to distinguish b/w fouts filename in OTF.
4. Enable the editor window for Embedded Mems so that user can enter any value into it.
5. Backend change for fuse locked parts in OCXO mode.
6. Fixed: Bug fix in using float instead of fraction for fout choices.
7. If the Gain mode is 1x fix Fin Internal limit to 4MHz.
8. Set a default value for VDD Output.
9. For BC1 Versions, VDD is set as default and greyed out from the user control.
10. For BC2 Versions, VDDIN is set as default and greyed out from the user control.
11. Fixed: BC1= VDDIO=VDD = 0x23[7] = 0 BC2=VDDIO=VDDIN = 0x23[7] =1. This was reversed and fixed correctly now.
12. Fix the XO frequency to 76.8 + 800 ppm.
13. Add 'Fuse Lock' to other variants: SiT95147, SiT95145, SiT95141.
14. Fixed: Assertion Error opening the GUI (SiT19541BC1 and BC2).
15. For DIVN and DIVN2 show INT, NUM, DEN in the Realtime window.
16. Maintain the Fout/Fin_internal to be an Integer relation whenever possible.
17. Fixed: Verify Efuse is not saving the mismatch file.
18. Fixed: LVDS2 and VDDO = 1.8V combination is not supported and an error message should be thrown when a customer uses this configuration.
19. Till 1.30.4 GUI, VDDIO register settings were defined as per RevC1, GUI release after that will support for RevC2 wafer only.
20. Removed BC1 And BC2 variants from the GUI and kept the flexibility to select VDDIO in the GUI.

18. Version 1.0032.9 [23-Jun-2023]

1. Fixed: Eliminated power-up registers checking during Verify E-Fuse.

2. Fixed: Added the possibility of the folder selection for the output file after Verify E-Fuse, instead of saving in the %temp folder.

3. Fixed: DCO from pins enabling changes the NVMs to actually enable the DCO from pins. Additionally disabled the DCO from pins mode in the SiT45148 GUI variant which does not support this function.

5. Fixed: Adding warning in case the SE driver settings are not finalized before the "Send to Chip".

6. Fixed: Added checking in the On-the-Fly mode to enter frequency in the valid range.

7. Fixed: Eliminated the possibility to assign the different frequencies to one PLL in the On-the-Fly mode.

8. Fixed: Fuse Lock support 2 PLLs at the same Frequency.

9. Fixed: Device E-Fuse not working in some cases

10. Added variant encoding for SiT9514x at page 1 register 0x2F[5:4]:

    1. SiT95141: 00b
    2. SiT95145: 01b
    3. SiT95147: 10b
    4. SiT95148: 11b.

11. Added part number encoding to the scratch memory space (for both *.nvm.py and *.efuse.nvm.py files). The part number can be entered as a number between 0 and 65,535 and encoded as a 16-bits binary representation of this number in the following memory space:

    1. Page 1 register 0x1E[7:3]
    2. Page 1 register 0x21[7:3]
    3. Page 1 register 0x27[7:3]
    4. Page 1 register 0x2b[7]

12. Added scratch memory access from the GUI. The user can now use scratch memory in the following memory space:

    1. Page 1 register 0x12[6:3]
    2. Page 1 register 0x18[7:4]
    3. Page 1 register 0x1b[7:4]
    4. Page 1 register 0x2e[7:4]

13. Added Fast Lock Holdover status displaying once Frequency Ramp selected/de-selected for user notifying.

14. Fixed: Real-time window issue with the continuous read and full information display. Additionally, fixed the issue with dividers display.

15. Fixed: Issue with manual input selection in the SiT95141 variant.

16. Fixed: Issue with the wrong warning: "Warning: There is FVCO XO Clash" for some SiT95148 configuration.

Table 4: Revision History

Version	Release Date	Change Summary
1.0	26-Jan-2021	Initial Release
1.05	19-Sep-2022	v1.0032.7 updates shown.
1.06	23-Jun-2023	v1.0032.9 updates shown.

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