

Description

The [SiT9505](#) is a differential oscillator with an integrated MEMS resonator (such as ApexMEMS™), that is engineered for low-jitter applications requiring one of the following standard frequencies: 50 MHz, 100 MHz, 156.25 MHz, 312.5 MHz, or 625 MHz.

In addition to standard differential signaling types, a unique FlexSwing™ output-driver performs like LVPECL and provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9505 can be factory programmed for specific combinations of frequency, stability, output signaling, voltage, and output enable functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Standard frequencies: 50 MHz, 100 MHz, 156.25 MHz, 312.5 MHz, 625 MHz
- 41 fs RMS typical phase jitter for SerDes applications
- 9 fs/mV typical PSNR
- LVPECL, LVDS, LVDS-2, LVDS-3, HCSL, Low-power HCSL, and FlexSwing signaling options
- ± 20 , ± 25 , ± 30 , and ± 50 ppm frequency stabilities
- Wide temperature range (-40°C to 105°C)
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous power supply voltage range options
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package

Applications

- 400G/800G network equipment
- Optical modules
- Coherent optics
- Network switches, routers



Block Diagram

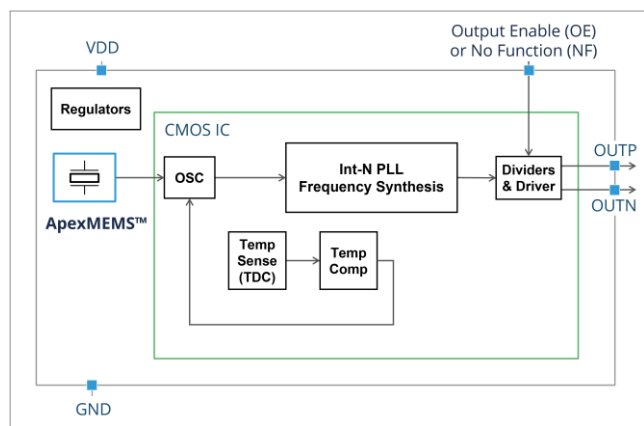


Figure 1. SiT9505 Block Diagram

Package Pinout

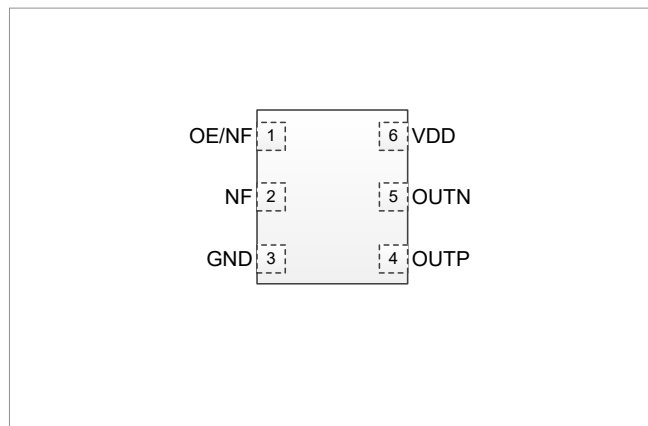


Figure 2. Pin Assignments (Top view)
(Refer to [Table 18](#) for Pin Descriptions)

SiT9505 features 41 fs RMS phase jitter for SerDes applications. Figure 3 shows the phase noise (green curve) observed by the system, after accounting for aliased phase noise when filtering (gray curve) the measured SiT9505 phase noise (blue curve). This “4-16A” phase jitter analysis methodology more accurately estimates reference clock

jitter than the legacy “12 kHz to 20 MHz” brick-wall filter methodology. It can be applied to all modern SerDes applications to optimize system performance. See “4-16A” [Phase Jitter Methodology for SerDes Applications](#) for more information.

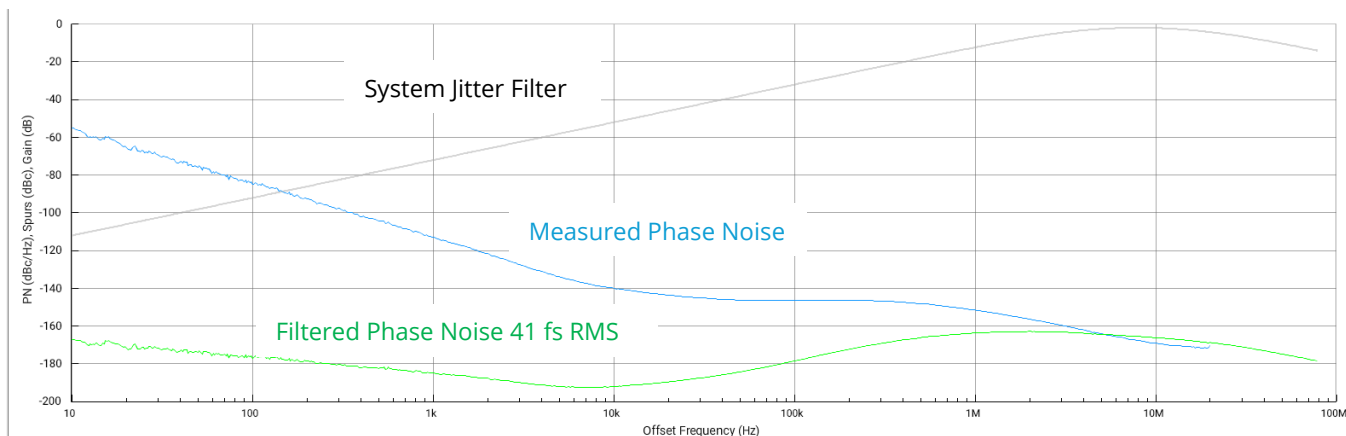
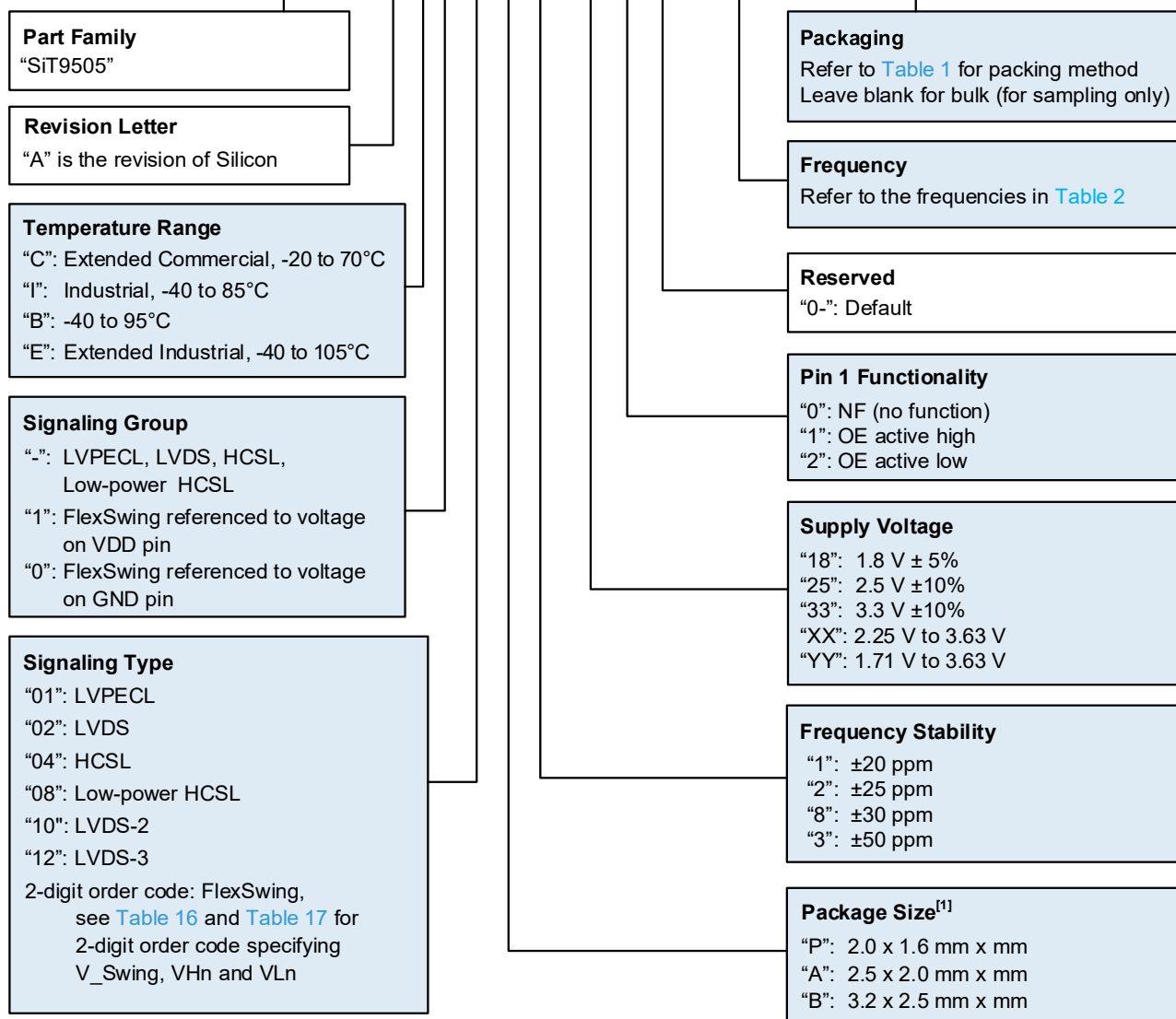


Figure 3. Phase noise before and after filtering for SiT9505 (156.25 MHz, LVPECL, 2.5 V, 25°C). The filter is applied to analyze phase noise with aliasing included up to the 3rd harmonic and features first-order filter cutoff frequencies of 4 MHz (high pass) and 16 MHz (low pass).

Ordering Information

SiT9505AC-01P2-3310-156.250000D



Note:

1. Contact SiTime for other package sizes.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

Table 2. Supported Frequencies

50.000000 MHz	100.000000 MHz	156.250000 MHz	312.500000 MHz	625.000000 MHz
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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage. See [Test Circuit Diagrams](#) for the test setups used with each signaling type.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 2 pF ±10%, and 10 years aging at 85°C
		–	–	±25	ppm	
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±0.7	±2.3	ppm	Ambient temperature of 85°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code “YY”
		2.25	–	3.63	V	Voltage-supply order code “XX”
		1.71	1.80	1.89	V	Voltage-supply order code “18”. Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code “25”
		2.97	3.30	3.63	V	Voltage-supply order code “33”
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Logic High function for Pin 1
Input Voltage Low	VIL	–	–	30%	Vdd	Logic High function for Pin 1
Input Pull-up/Pull-down Impedance	Z_in	112.9	120	133.4	kΩ	Pin 1 for OE function
Output Characteristics						
Duty Cycle	DC	48	–	52	%	See Figure 21 for waveform
Startup, OE and SE Timing						
Startup Time	T_start	–	1.2	2	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time 1	T_oe	–	–	100+3 clock cycles	ns	For all signaling types except Low-Power HCSSL. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 27 for waveform
Output Enable Time 2	T_oe	–	–	500+3 clock cycles	ns	For Low-Power HCSSL signaling type. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 27 for waveform
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 28 for waveform
Period Jitter, Cycle-to-cycle Jitter and Spurious Phase Noise						
Legacy Spurious Phase Noise	T_spn	–	–	-110	dBc	12 kHz to 20 MHz offset frequency range
RMS Period Jitter ^[3]	T_jitt_per	–	0.5	0.6	ps	Measured based on 10K cycles
Peak Cycle-to-cycle Jitter ^[3]	T_jitt_cc	–	3.5	6.2	ps	Measured based on 1K cycles

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter and Phase Noise, measured at f = 156.25 MHz						
4-16A Phase Jitter^[2]	T_416A	–	41	52 ^[4]	fs RMS	Measured with phase noise analyzer, extending (flat) phase noise to 3rd harmonic (i.e., 312.5 MHz offset), folding phase noise below the Nyquist frequency (i.e., 78.125 MHz offset), filtering and integrating from 10 kHz to Nyquist. Uses 4 MHz high pass and 16 MHz low pass filters, each with 20 dB/dec roll off. Includes spurs. See “4-16A” Phase Jitter Methodology for SerDes Applications for additional details.
0.012-20 Phase Jitter (legacy)	T_phj	–	72	100	fs RMS	Measured with phase noise analyzer, integrating between 12 kHz and 20 MHz offset frequency. Recommended for SONET OC-48 applications. Contact SiTime for 85 fs max option.
0.012-20 Phase Jitter (with 4MHz HPF)	T_phj	–	28	34	fs RMS	Measured with phase noise analyzer, filtering and integrating from 12 kHz to 20MHz. Uses 4 MHz high pass and 20 MHz low pass filters, each with 20 dB/dec roll off. Includes spurs.
Phase Noise – 1KHz offset		–	-113	-106	dBc/Hz	
Phase Noise – 10KHz offset		–	-140	-136	dBc/Hz	
Phase Noise – 100KHz offset		–	-147	-144	dBc/Hz	
Phase Noise – 1MHz offset		–	-152	-150	dBc/Hz	
Phase Noise – 10MHz offset		–	-169	-167	dBc/Hz	
Jitter and Phase Noise, measured at f = 312.5 MHz						
0.012-20 Phase Jitter (legacy)	T_phj	–	73	100	fs RMS	Measured with phase noise analyzer, integrating between 12 kHz and 20 MHz offset frequency. Recommended SONET OC-48 applications.
0.012-20 Phase Jitter (with 4MHz HPF)	T_phj	–	29	39	fs RMS	Measured with phase noise analyzer, filtering and integrating from 12 kHz to 20MHz. Uses 4 MHz high pass and 20 MHz low pass filters, each with 20 dB/dec roll off. Includes spurs.
Phase Noise – 1KHz offset		–	-107	-100	dBc/Hz	
Phase Noise – 10KHz offset		–	-134	-130	dBc/Hz	
Phase Noise – 100KHz offset		–	-140	-138	dBc/Hz	
Phase Noise – 1MHz offset		–	-144	-143	dBc/Hz	
Phase Noise – 10MHz offset		–	-162	-161	dBc/Hz	

Note:

2. Recommended for SerDes applications to improve the accuracy of clock jitter analysis, replacing the traditional 12 kHz to 20 MHz brick wall filter when application-specific filter characteristics are not explicitly specified.
3. Measured according to JESD65B using Keysight DSAX91604A Oscilloscope.
4. Max phase jitter for LVPECL.

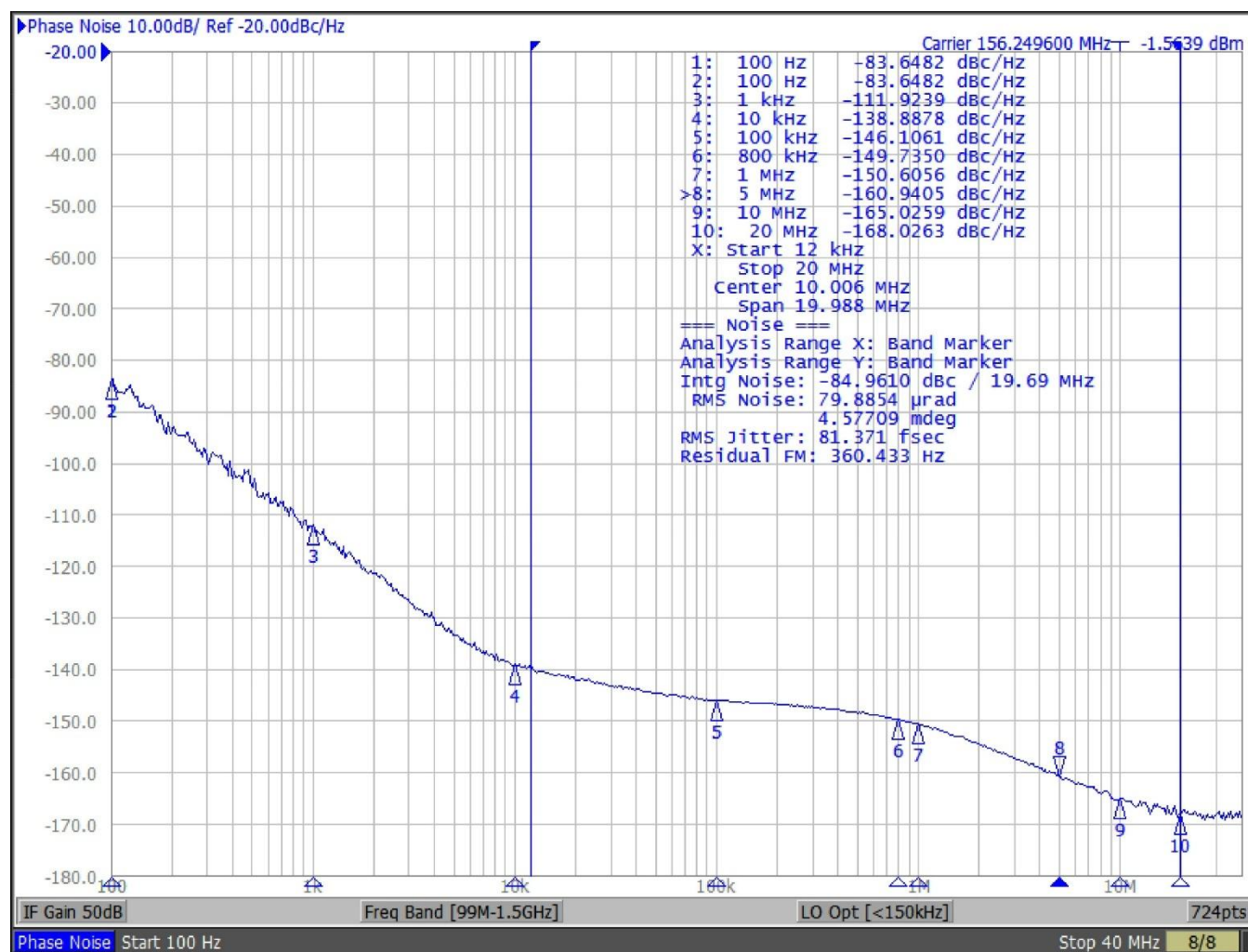


Figure 4. Phase Noise for 156.25 MHz output frequency (LVDS) measured at 25°C, 3.3V

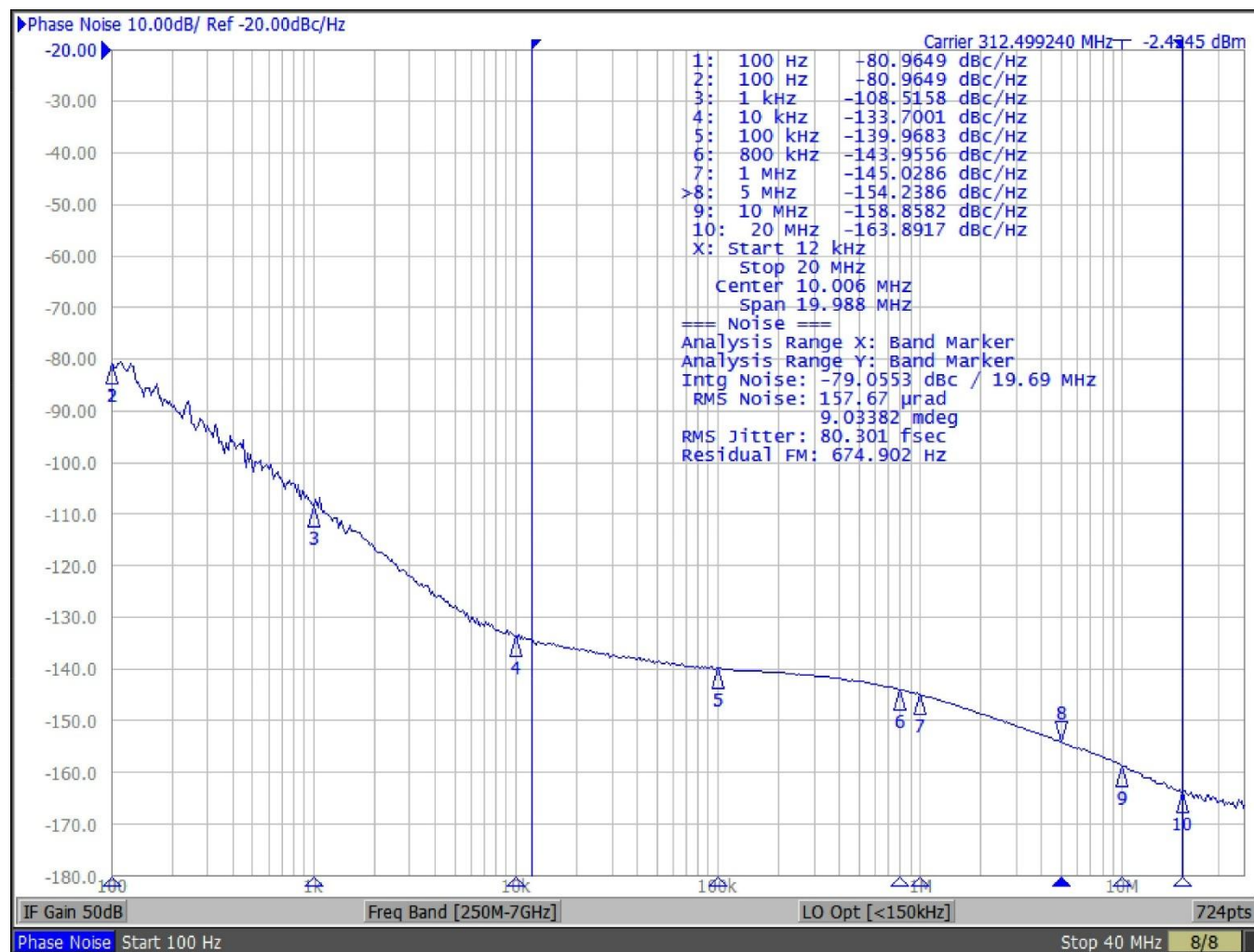


Figure 5. Phase Noise for 312.5MHz output frequency (LVDS) measured at 25°C, 3.3 V

Table 4. Electrical Characteristics – LVPECL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply voltage of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 10](#) and [Figure 11](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	35.5	42.5	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	46	56	mA	Including load termination current as shown in Figure 32 for Vdd=3.3 V $\pm 10\%$, Vdd=2.25 V to 3.63 V and R3=220 Ohms
		–	46	52	mA	Including load termination current as shown in Figure 32 for Vdd=2.5 V $\pm 10\%$ and R3=220 Ohms
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	62	68	mA	Including load termination current. See Figure 33 for termination
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	53.5	65	mA	Including load termination current as shown in Figure 32 for Vdd=3.3 V $\pm 10\%$, Vdd=2.25 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	53.5	60.5	mA	Including load termination current as shown in Figure 32 for Vdd=2.5 V $\pm 10\%$ and R3=220 Ohms. Driver output is at logic-high voltage levels.
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	73	80	mA	Including load termination current. See Figure 33 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.075	Vdd-0.95	Vdd-0.86	V	See Figure 20 for waveform
Output Low Voltage	VOL	Vdd-1.84	Vdd-1.7	Vdd-1.62	V	See Figure 20 for waveform
Output Differential Voltage Swing	V_Swing	1.4	1.5	1.65	V	See Figure 21 for waveform
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	45	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	± 30	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 25 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	9	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	2.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 10
Power Supply-Induced Phase Noise	PSIPN	–	-79	–	dBc	50 mV peak-peak ripple on VDD
		–	-92	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 10

Table 5. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to VDD only: 2.5 V $\pm$ 10% (“25”), 3.3 V $\pm$ 10% (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 12](#) and [Figure 13](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	36.5	45	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44	55	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 32 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms
		–	44	51	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 32 for Vdd=2.5 V ±10%, and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	49.5	60.5	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 32 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	49.5	57	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 32 for Vdd=2.5 V ±10%, and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn -0.13	VHn	VHn +0.1	V	See Figure 20 for waveform; Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn -0.13	VLn	VLn +0.12	V	See Figure 20 for waveform; Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 21 for waveform
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 25 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “ER”
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “ER”. Using RC power supply filter as shown in Figure 12
Power Supply-Induced Phase Noise	PSIPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “ER”
		–	-93	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “ER”. Using R C power supply filter as shown in Figure 12

Table 6. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 12](#) and [Figure 13](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	38	45	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	45.5	51	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 32 for Vdd=1.8 V ±5% and R3=220 Ohms
		–	45.5	52.5	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 32 for Vdd=1.71 V to 3.63 V and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	51.5	57.5	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 32 for Vdd=1.8 V ±5% and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	51.5	59	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 32 for Vdd=1.71 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.12	V	See Figure 20 for waveform; Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.12	V	See Figure 20 for waveform; Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 21 for waveform
Rise/Fall Time	Tr, Tf	–	170	210	ps	20% to 80%. See Figure 21 for waveform.
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 25 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	12	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “3E”
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “3E”. Using RC power supply filter as shown in Figure 12
Power Supply-Induced Phase Noise	PSIPN	–	-76	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “3E”
		–	-95	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “3E”. Using RC power supply filter as shown in Figure 12

Table 7. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 12](#) and [Figure 13](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	37	43	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44.5	51	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 32 for Vdd=3.3 V $\pm 10\%$, Vdd=2.25 V to 3.63 V, and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	53	61	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 32 for Vdd=3.3 V $\pm 10\%$, Vdd=2.25 V to 3.63 V, and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.11	VHn	VHn + 0.1	V	See Figure 20 for waveform; Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 20 for waveform; Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 21 for waveform
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	± 40	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 25 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “VP”
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code “VP”. Using RC power supply filter as shown in Figure 12
Power Supply-Induced Phase Noise	PSIPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “VP”
		–	-93	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code “VP”. Using RC power supply filter as shown in Figure 12

Table 8. Electrical Characteristics – LVDS-3 | Supply voltage (“order code”): 1.8 V $\pm$ 5% (“18”), 2.5 V $\pm$ 10% (“25”), 3.3 V $\pm$ 10% (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 14](#) and [Figure 15](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	41	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44	–	mA	Including load termination current. See Figure 35 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	50	–	mA	Including load termination current. See Figure 35 for termination. Driver output is at logic-high voltage levels.
Output Characteristics (AC-Coupled)						
Differential Output Voltage	VOD	400	–	800	mV	See Figure 22 for waveform, using Figure 35 for termination.
Rise/Fall Time	Tr, Tf	–	170	–	ps	Measured 20% to 80% using Figure 35 for termination. See Figure 21 for waveform.
Differential Asymmetry, peak-peak	V_da	–	90	–	mV	See Figure 23 for waveform, using Figure 35 for termination.
Differential Skew, peak	V_ds	–	$\pm$ 50	–	ps	See Figure 24 for waveform, using Figure 35 for termination.
Overshoot Voltage, peak	V_ov	–	18	–	%	Measured as percent of VOD. See Figure 26 for waveform, using Figure 35 for termination.

Table 9. Electrical Characteristics – LVDS-2 | Supply voltage (“order code”): 1.8 V $\pm 5\%$ (“18”), 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 14](#) and [Figure 15](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	41	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44	–	mA	Including load termination current. See Figure 35 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	50	–	mA	Including load termination current. See Figure 35 for termination. Driver output is at logic-high voltage levels.
Output Characteristics (AC-Coupled)						
Differential Output Voltage	VOD	300	–	600	mV	See Figure 22 for waveform, using Figure 35 for termination.
Rise/Fall Time	Tr, Tf	–	170	–	ps	Measured 20% to 80% using Figure 35 for termination. See Figure 21 for waveform.
Differential Asymmetry, peak-peak	V_da	–	65	–	mV	See Figure 23 for waveform, using Figure 35 for termination.
Differential Skew, peak	V_ds	–	± 50	–	ps	See Figure 24 for waveform, using Figure 35 for termination.
Overshoot Voltage, peak	V_ov	–	19	–	%	Measured as percent of VOD. See Figure 26 for waveform, using Figure 35 for termination.

Table 10. Electrical Characteristics – LVDS | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 14](#) and [Figure 15](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32.5	39	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	36	42	mA	Including load termination current. See Figure 36 for termination
Current Consumption Output Disabled with Termination	Idd_od_wt	–	42	48	mA	Including load termination current. See Figure 36 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	360	450	mV	See Figure 22 for waveform
Delta VOD	ΔVOD	–	–	50	mV	See Figure 22 for waveform
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 22 for waveform
Delta VOS	ΔVOS	–	–	50	mV	See Figure 22 for waveform
Rise/Fall Time	Tr, Tf	–	290	330	ps	Measured 20% to 80% using Figure 36 for termination. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	± 40	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of VOD. See Figure 26 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	15	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
	PSIJS	–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 14
Power Supply-Induced Phase Noise	PSIPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD
	PSIPN	–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 14

Table 11. Electrical Characteristics – LVDS | Supply voltage (“order code”): 1.8 V $\pm$ 5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 14](#) and [Figure 15](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32.5	39	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	36	42	mA	Including load termination current. See Figure 35 and Figure 36 for termination
Current Consumption Output Disabled with Termination	Idd_od_wt	–	41.5	48	mA	Including load termination current. See Figure 35 and Figure 36 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	330	450	mV	See Figure 22 for waveform
Delta VOD	Δ VOD	–	–	50	mV	See Figure 22 for waveform
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 22 for waveform
Delta VOS	Δ VOS	–	–	50	mV	See Figure 22 for waveform
Rise/Fall Time	Tr, Tf	–	290	330	ps	Measured 20% to 80% using Figure 36 for termination. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	$\pm$ 40	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of VOD. See Figure 26 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	17.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 14
Power Supply-Induced Phase Noise	PSIPN	–	-73	–	dBc	50 mV peak-peak ripple on VDD
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 14

Table 12. Electrical Characteristics – HCSL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 16](#) and [Figure 17](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32	38	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	46.5	52	mA	Including load termination current. See Figure 37 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	52.5	59	mA	Including load termination current. See Figure 37 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 20 for waveform
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 20 for waveform
Output Differential Voltage Swing	V_Swing	1.1	1.4	1.6	V	See Figure 21 for waveform
Rise/Fall Time	Tr, Tf	–	340	370	ps	Measured 20% to 80%. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	65	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	± 70	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	0	–	%	Measured as percent of V_Swing. See Figure 25 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	27	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 16
Power Supply-Induced Phase Noise	PSIPN	–	-70	–	dBc	50 mV peak-peak ripple on VDD
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 16

Table 13. Electrical Characteristics – Low-Power HCSL | Supply voltage (“order code”): 2.5 V $\pm$ 10% (“25”), 3.3 V $\pm$ 10% (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V $\pm$ 5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See [Figure 18](#) and [Figure 19](#) for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	33	38.5	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	33.5	39	mA	Including load termination current. See Figure 38 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	35.5	42	mA	Including load termination current. See Figure 38 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.92	1.15	V	See Figure 20 for waveform
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 20 for waveform
Output Differential Voltage Swing	V_Swing	1.6	1.83	2.0	V	See Figure 21 for waveform
Rise/Fall Time	Tr, Tf	–	330	380	ps	Measured 20% to 80%. See Figure 21 for waveform
Differential Asymmetry, peak-peak	V_da	–	55	–	mV	See Figure 23 for waveform
Differential Skew, peak	V_ds	–	$\pm$ 30	–	ps	See Figure 24 for waveform
Overshoot Voltage, peak	V_ov	–	1	–	%	Measured as percent of V_Swing. See Figure 25 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSIJS	–	18	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	6.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 18
Power Supply-Induced Phase Noise	PSIPN	–	-73	–	dBc	50 mV peak-peak ripple on VDD
		–	-82	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 18

Table 14. Absolute Maximum Ratings

Operation outside the absolute maximum ratings may cause permanent damage to the part.
Performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	135	°C

Table 15. Thermal Considerations^[5]

Package	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	θ_{JB} (°C/W)	$\theta_{JC,Top}$ (°C/W)
3225, 6-pin	111	5.1	34	86
2520, 6-pin	126	4.8	39	118
2016, 6-pin	149	3.9	40	163

Notes:

5. θ_{JA} , Ψ_{JT} , θ_{JB} and θ_{JC} are provided according to JEDEC standards 51-2A, 51-7, 51-8, and 51-12.01 with a 25°C ambient and 250 mW power consumption (typical of 1 GHz f_{out}). The conduction thermal resistances θ_{JB} and θ_{JC} are obtained with the assumption that all heat flows from the junction to a heat sink through either the solder pads (θ_{JB}) or the top of the package ($\theta_{JC,Top}$). These may be used in a two-resistor compact model. The values of θ_{JA} and Ψ_{JT} are strongly application dependent, and we report values based on the JEDEC thermal environment. θ_{JA} is the thermal resistance to ambient on a JEDEC PCB - it is a highly conservative estimate, since the JEDEC board does not have vias to PCB planes in the vicinity of the package. Ψ_{JT} can be used to estimate the junction temperature from measurements of the temperature at the top of the package if the thermal environment is similar to the JEDEC environment.

Table 16. Maximum Operating Junction Temperature^[6]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80°C
85°C	95°C
95°C	105°C
105°C	115°C

Notes:

6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 17. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	<i>g</i>
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	<i>g</i>
Soldering Temperature (follow standard Pb free soldering guidelines) ^[7]	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

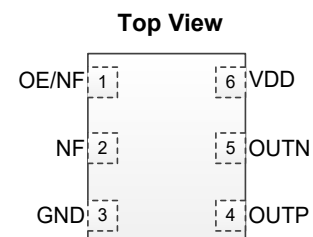
Notes:

7. Please refer to [SiTime Manufacturing Notes](#).

Pin Description

Table 18. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H ^[8] : Specified frequency output L ^[9] : OUT: Logic HIGH,
		No Function (NF)	Open, 120 kΩ internal pull-down resistor to GND
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions. ^[10]
3	GND	Power	Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[8]


Figure 6. Pin Assignments
Notes:

8. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, the OE pin is recommended to include an external 10 kΩ resistor (Use 10 kΩ pull-up if active high OE; use 10 kΩ pull-down if active low OE) when the pin is not externally driven.
9. Differential Logic high means OUTP=VOH, OUTN=VOL
10. Can be left open. SiTime recommends grounding it for better thermal performance.
11. A capacitor of value 0.1 μF or higher between VDD and GND pins is required.

“4-16A” Phase Jitter Methodology for SerDes Applications

Proper evaluation of reference clock (refclk) jitter is critical to optimize system performance in high-speed serial links.

Figure 7 shows how the traditional 12 kHz to 20 MHz analysis of filtering refclk jitter can mislead designers to

select components that degrade rather than improve link performance. Using a more accurate filter analysis predicts a 50% reduction (41 vs 94 fs RMS) in jitter. Therefore, this datasheet replaces the legacy 12 kHz to 20 MHz filter analysis with a more accurate and established methodology adopted by several industry standards (e.g. PCI Express, CXL, UCIe) and implemented here as “4-16A” phase jitter. A brief overview follows.

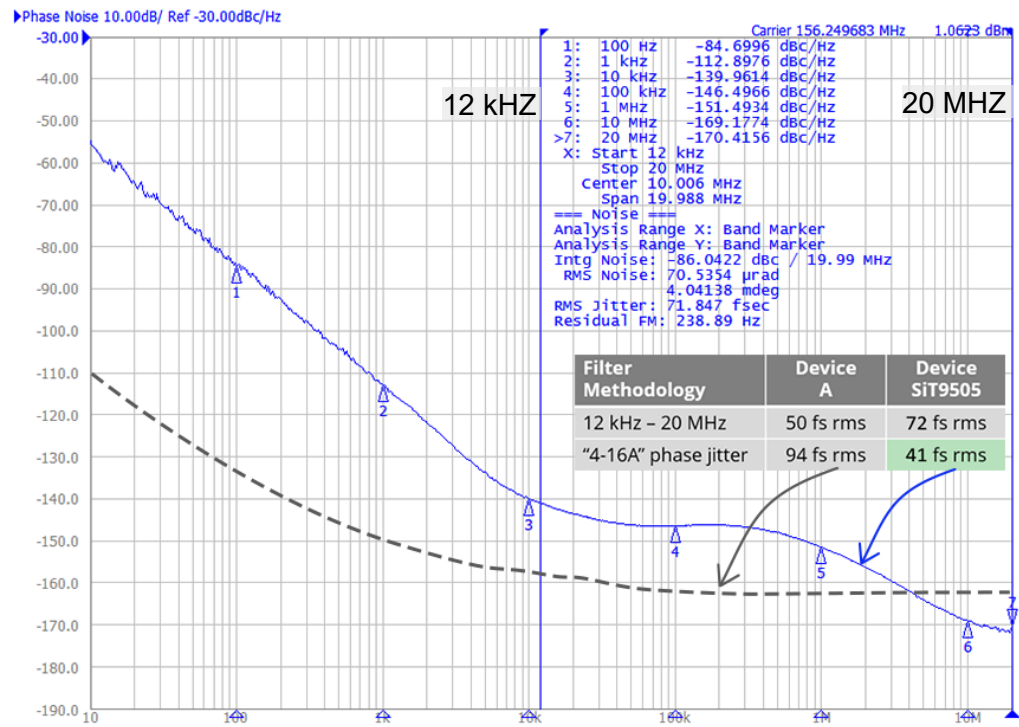


Figure 7. Two products analyzed with 2 different methodologies lead to opposite conclusions. The “4-16A” phase jitter methodology more accurately predicts in-system performance for modern SerDes applications.

Established in 1991 for SONET OC-48 line rates, the traditional 12 kHz to 20 MHz jitter filter served as a golden reference to evaluate refclk jitter for over 30 years. The filter is used is nearly all clock and timing datasheets today. However, the results it provides no longer correlate with system performance and can create suboptimum link performance. Sources of filter error include incorrect corner frequencies, unrealistic brick-wall roll offs and a lack of accounting for aliased phase noise. Errors of tens of femtoseconds are significant today and will become more significant as data rates increase. For these reasons, we recommend customers adopt the more accurate “4-16A” phase jitter methodology for SerDes applications.

The conventional refclk jitter analysis uses a band-pass filter, as shown in Figure 8, to extract the refclk contribution to jitter observed at the receiver. Historically the refclk jitter filter was arbitrarily applied to phase noise up to an offset equal to the refclk Nyquist frequency. However, this ignores higher-offset phase noise that aliases when the refclk is sampled by a PLL’s digital phase detector. Studies have shown that extending the measured phase noise data flat to the third harmonic (or, twice the fundamental frequency in the offset-frequency axis) accurately estimates worst-case phase jitter¹². Above the third harmonic, phase noise rolls off quickly and can be ignored.

Note:
12. “How to evaluate reference-clock phase noise in high-speed serial links”, Signal Integrity Journal (May 3, 2019).

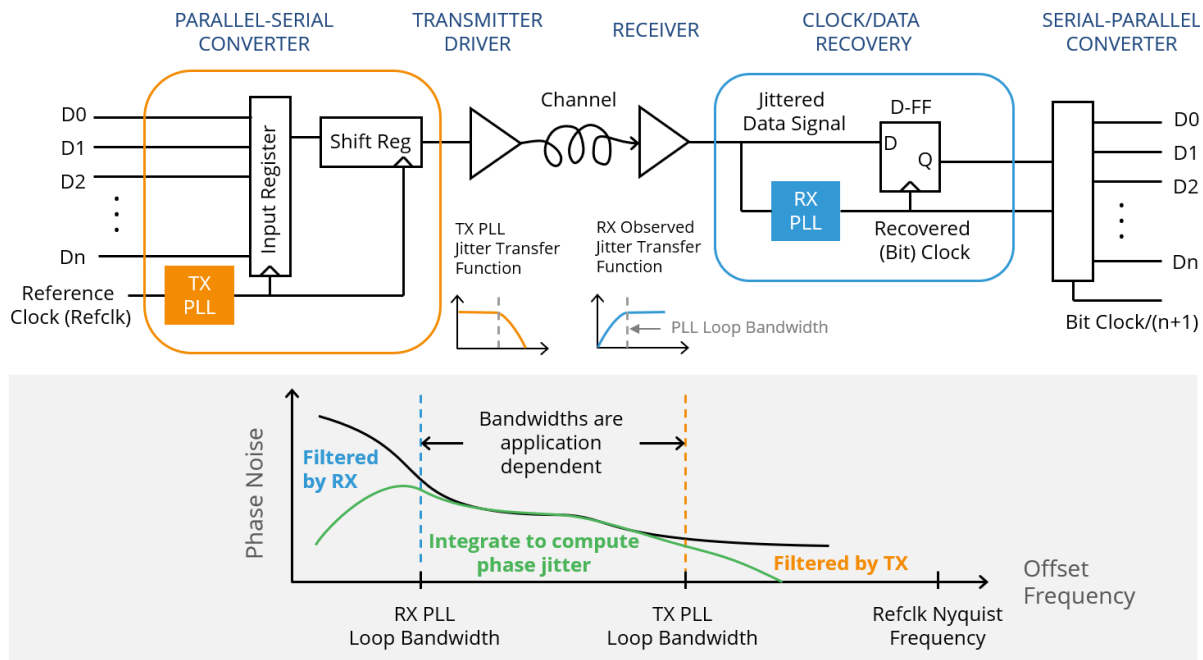


Figure 8. A generic serial link (top) uses a transmit PLL and receive CDR to low and high pass filter, respectively, refclk phase noise. This forms a band-pass system filter (bottom) for computing phase jitter.

The left **Figure 9** chart illustrates this methodology of filtering aliased phase noise for a 156.25 MHz clock. Direct phase noise analyzer instruments (e.g., E5052B or FSWP) include an anti-aliasing filter. Thus, to account for aliasing, the phase noise is extended flat to the 3rd harmonic (468.75 MHz in the signal spectrum, or 312.5 MHz in offset frequency spectrum) and the jitter filter is folded across

Nyquist-zone boundaries (at 156.25/2, 156.25 and 156.25×3/2 MHz). Then the phase noise data is filtered and integrated to derive phase jitter. The right chart in **Figure 9** illustrates a mathematically equivalent process that aliases the extended phase noise below an offset equal to the Nyquist frequency before filtering in the first Nyquist zone^[12].

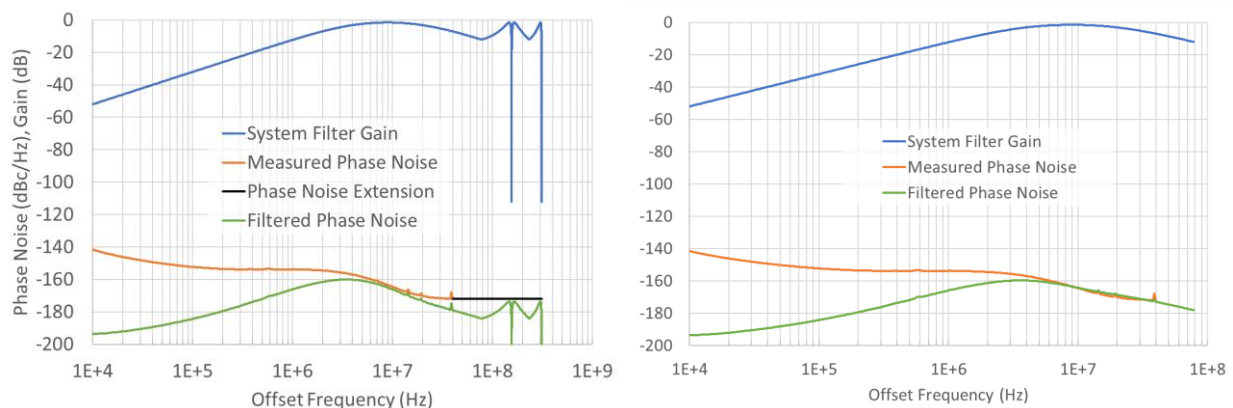


Figure 9. Illustration of two equivalent processes to filter aliased phase noise. The left chart extends (black) the measured phase noise (orange) to the 3rd harmonic, mirrors the filter (blue) across higher Nyquist zones before deriving the filtered phase noise (green). Alternatively, the right chart aliases the extended phase noise (not shown) below the Nyquist frequency before filtering (green). Integrating either green curve produces the same phase jitter.

A shorthand label for this methodology is “#-#A” phase jitter where the first and second numbers “#” are replaced with RX CDR and TX PLL bandwidths, respectively, and assuming 20 dB/dec roll offs (unless specified otherwise), and “A” indicates that aliasing is included. For example, “4-16A” phase jitter uses 4 MHz RX and 16 MHz TX bandwidths with aliasing. Here, 4 MHz represents the most common serial standard, Ethernet, which typically specifies a CDR bandwidth of 4 MHz for 10 Gbps and higher link

rates, and 16 MHz represents a worst-case estimate for TX PLL bandwidth (the PLL becomes unstable at higher bandwidths). This shorthand terminology makes it easy to describe variations. For example, “2-10A” phase jitter describes the same methodology but for 2 MHz RX CDR and 10 MHz TX PLL bandwidths. In practice, the exact bandwidths are application dependent, and “4-16A” is simply chosen here to represent the most common application (Ethernet).

Table 20. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on GND pin

Order Code V_Swing (V)		C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y
		0.45V	0.49V	0.54V	0.59V	0.64V	0.69V	0.74V	0.79V	0.84V	0.89V	0.94V	0.99V	1.03V	1.08V	1.16V	1.23V	1.3V	1.38V	1.45V	1.53V	1.6V
VHn	A																		AV	AW	AX	AY
	B																		1.94	1.86	1.69	1.61
	C																		CU	CV	CW	CX
	D																		1.94	1.77	1.69	1.52
	E																		DT	DU	DV	DX
	F																		1.94	1.86	1.69	1.44
	G																		ET	EU	EV	EY
	H																		1.86	1.77	1.61	1.27
	J																		FS	FT	FW	FY
	K																		1.94	1.77	1.69	1.18
	L																		GS	GT	GU	GY
	M																		1.94	1.86	1.61	1.10
	N																		HS	HT	HV	HY
	P																		1.77	1.61	1.52	1.01
	Q																		JS	JT	JU	JY
	R																		1.69	1.52	1.44	0.93
	S																		KS	KT	KV	KY
	T																		1.94	1.86	1.77	0.85
	U																		LS	LT	LU	LY
	V																		1.52	1.35	1.27	0.76
	W																		MR	MS	MT	MY
	X																		1.52	1.44	1.27	0.68
	Y																		NQ	NR	NS	NY
	Z																		1.94	1.86	1.77	0.59
	1																		PP	PQ	PR	PY
	2																		1.94	1.86	1.77	0.51
	3																		QN	QP	QQ	QY
																			1.52	1.44	1.35	0.42
																			RM	RN	RP	
																			1.27	1.18	1.10	0.34
																			SL	SM	SN	0.25
																			1.94	1.86	1.77	
																			TK	TL	TM	
																			1.94	1.86	1.77	
																			UJ	UK	UL	
																			1.94	1.86	1.77	
																			VH	VJ	VK	
																			1.94	1.86	1.77	
																			WG	WH	WJ	
																			1.86	1.77	1.69	
																			XF	XG	XH	
																			1.77	1.69	1.61	
																			YE	YF	YG	
																			1.69	1.61	1.52	
																			ZD	ZE	ZF	
																			1.61	1.52	1.44	
																			1C	1D	1E	
																			1.52	1.44	1.35	
																			2C	2D	2E	
																			1.44	1.35	1.27	
																			3C	3D	3E	
																			1.35	1.27	1.18	

Note:

15. Please [contact SiTime](#).

Test Circuit Diagrams

A 1.5 pF capacitive load is used at each differential output. Because of the additive input capacitance of the active probe used with the oscilloscope, the output characteristics for all signal types are measured with a total of 2 pF capacitive load.

Test Setups for LVPECL Measurements

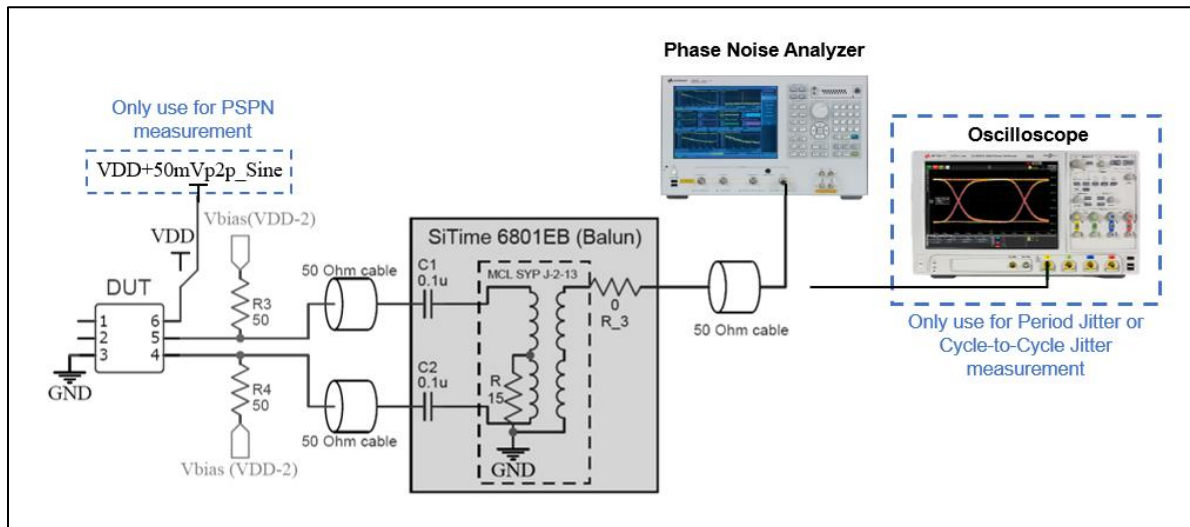


Figure 10. Test setup to measure LVPECL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSIPN) without filter added^[16]

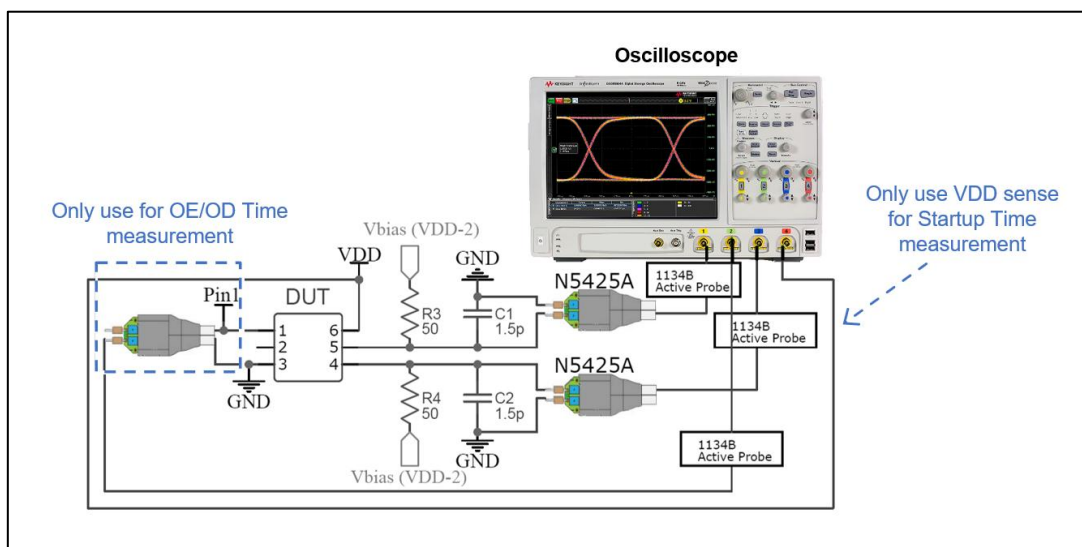


Figure 11. Test setup to measure LVPECL Waveform Characteristics, Current Consumption (with Termination 2)^[17], Output Enable/Disable Time, and Startup Time

Notes:

16. See Figure 12 for the test setup to measure LVPECL Power Supply-Induced Phase Noise (PSIPN) with filter added.
17. See Figure 13 for the test setup to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for LVDS Measurements

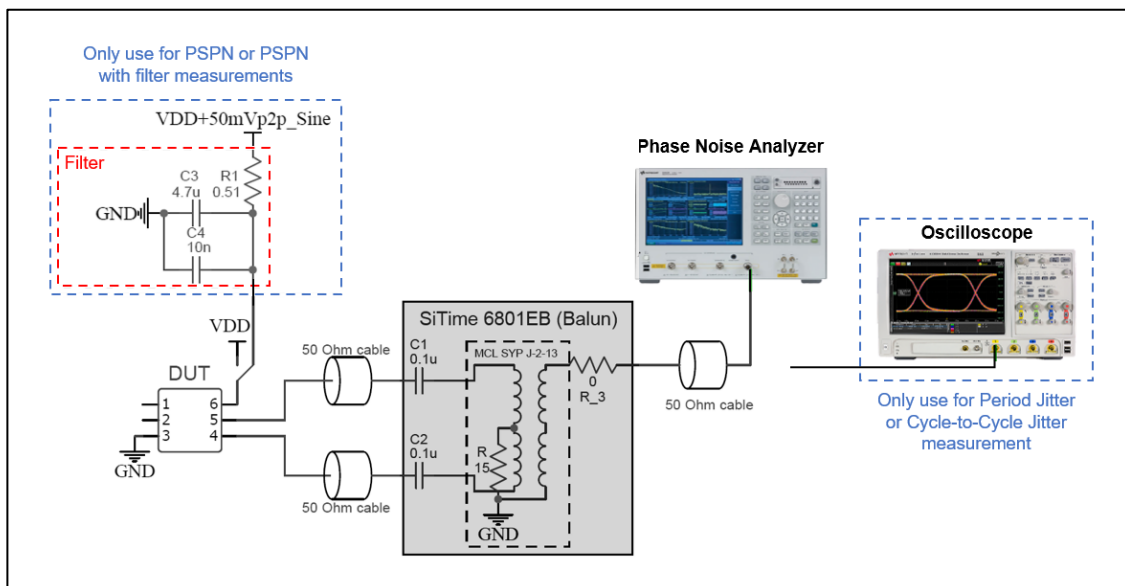


Figure 14. Test setup to measure LVDS Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSIPN) with and without filter added

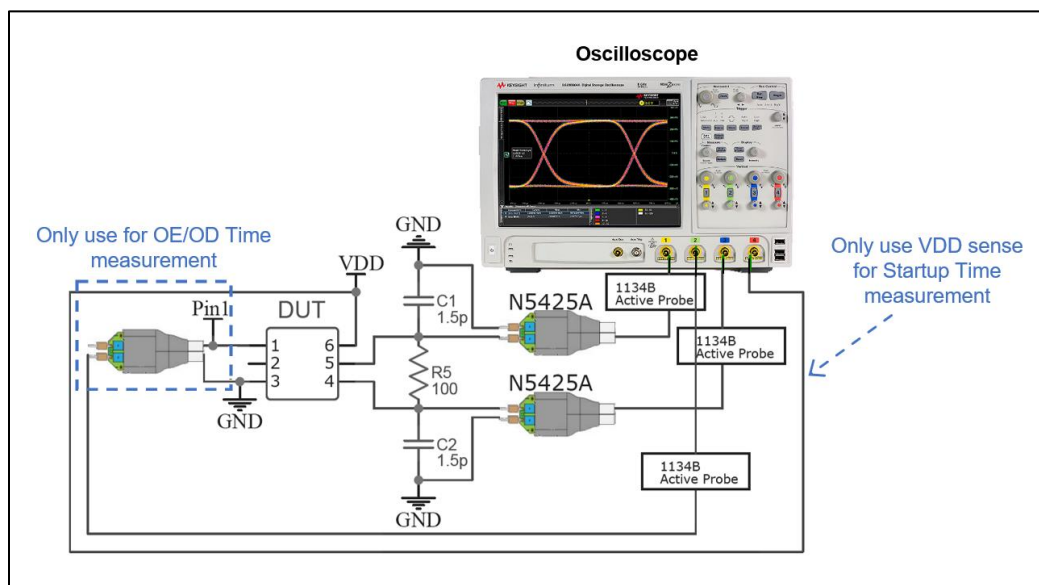
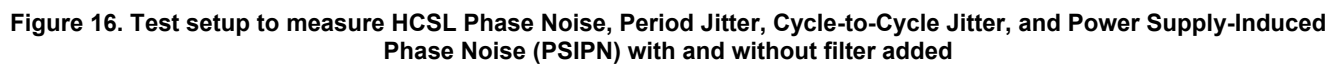
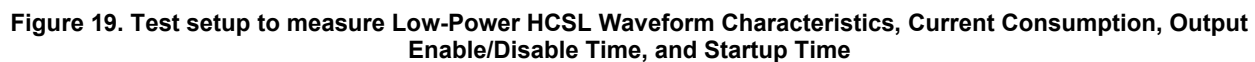


Figure 15. Test setup to measure LVDS Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Setups for HCSL Measurements



Test Setups for Low-Power HCSL Measurements



Waveform Diagrams

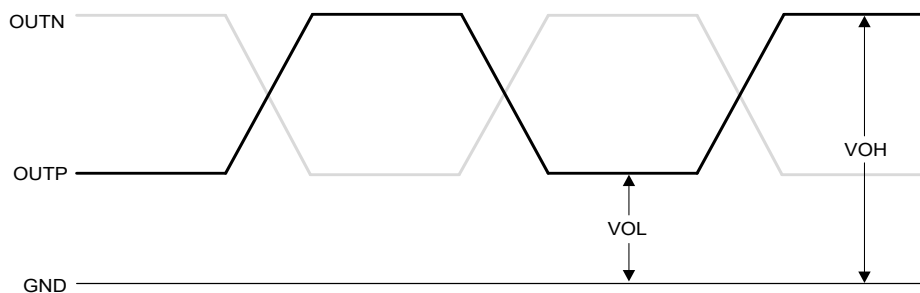


Figure 20. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

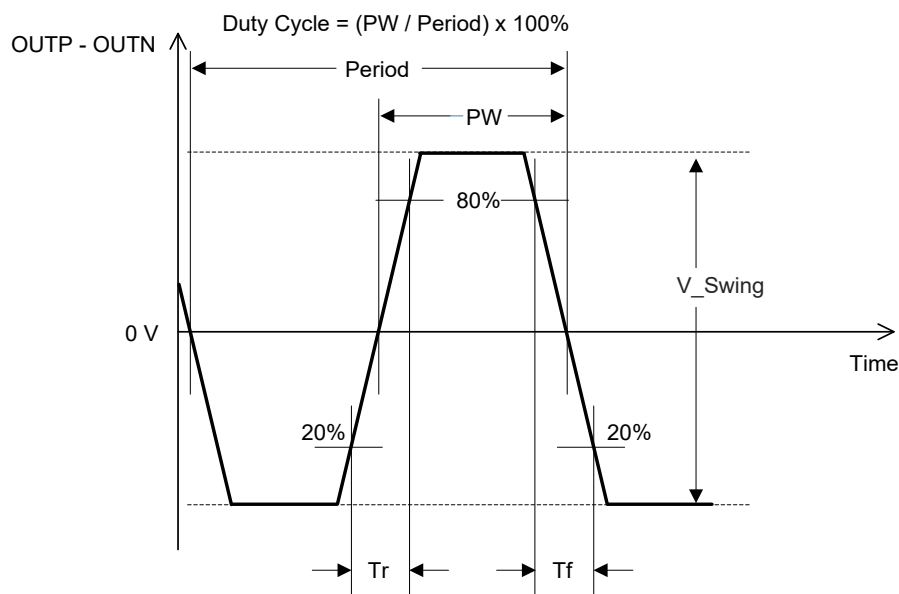


Figure 21. LVPECL, LVDS, LVDS-2, LVDS-3, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

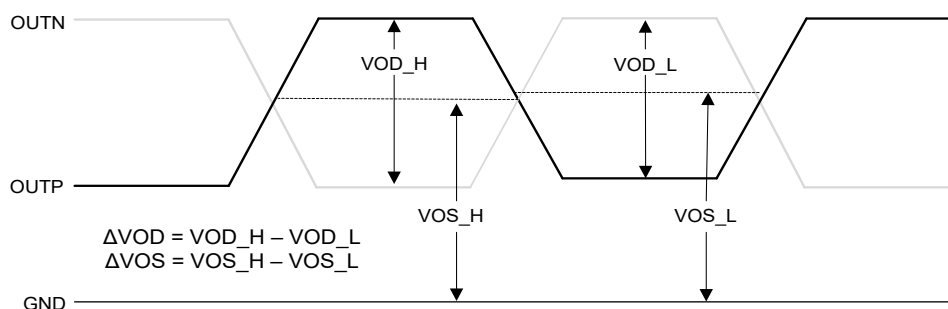


Figure 22. LVDS, LVDS-2, LVDS-3 Voltage Levels per Differential Pin

Waveform Diagrams (continued)

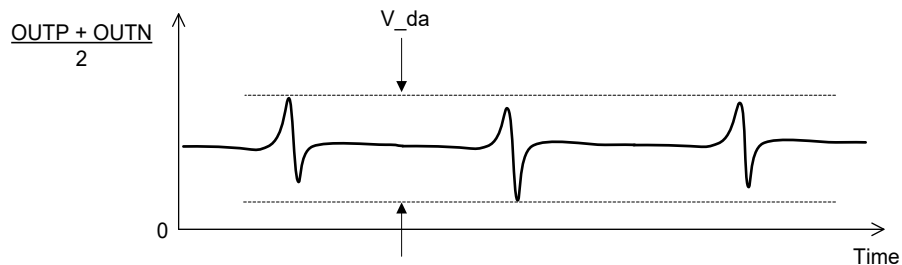


Figure 23. Differential Asymmetry (V_{da})

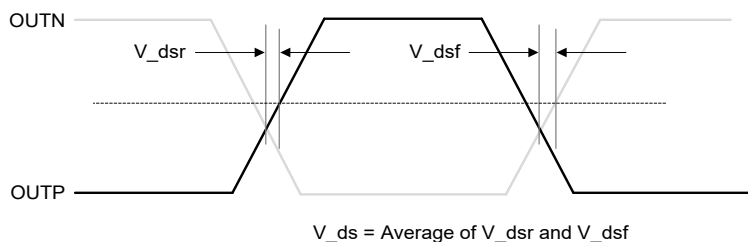


Figure 24. Differential Skew (V_{ds}) is measured as the Time between the Average Voltage Level and Crossing Voltage

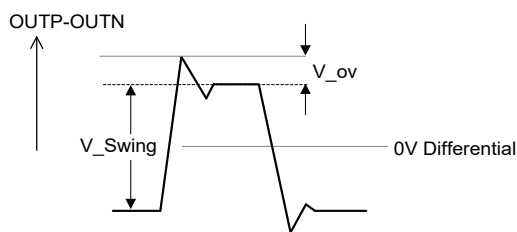


Figure 25. Overshoot Voltage (V_{ov}) for LVPECL, FlexSwing, HCSL, Low-power HCSL

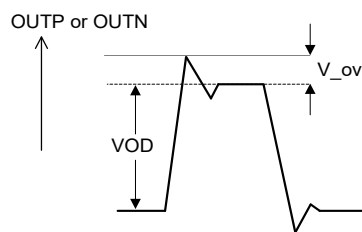


Figure 26. Overshoot Voltage (V_{ov}) for LVDS, LVDS-2, LVDS-3 Output

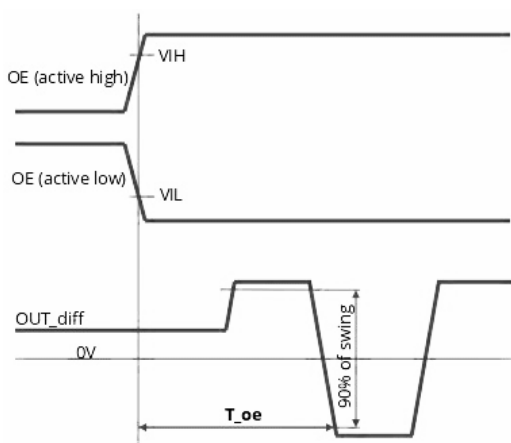


Figure 27. OE Pin Enable Timing (T_{oe})

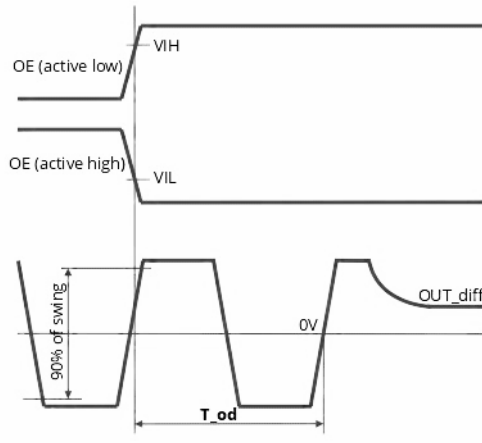


Figure 28. OE Pin Disable Timing (T_{od})

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9505 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in Figure 30 and Figure 32, compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are

voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_{load}) into the load termination.

Table 21. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage Order Codes	Termination Options					
		Figure 29	Figure 30	Figure 31	Figure 32	Figure 33	Figure 34
LVPECL referenced to Vdd	"25", "33", "XX"	OK to use $I_{load} = 40\text{ mA}$ with $100\ \Omega$ near-end bias resistor	Do Not Use	OK to use $I_{load} = 28\text{ mA}$	OK to use	OK to use $I_{load} = 28\text{ mA}$	Do Not Use
FlexSwing referenced to Vdd		OK to use ²¹	OK to use (see Figure 30 for frequency ranges and voltage swings)	OK to use ²²	OK to use	OK to use	Do Not Use
FlexSwing referenced to Gnd	"25", "33", "XX", "YY"			Do Not Use	OK to use	Do Not Use	Do Not Use
	"18"			Do Not Use	OK to use	Do Not Use	OK to use

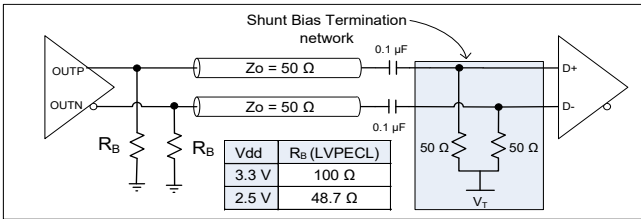


Figure 29. Recommended LVPECL and FlexSwing^[21] Termination when AC-coupled

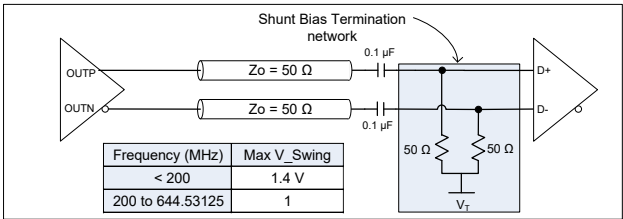


Figure 30. Recommended FlexSwing Termination when AC-coupled

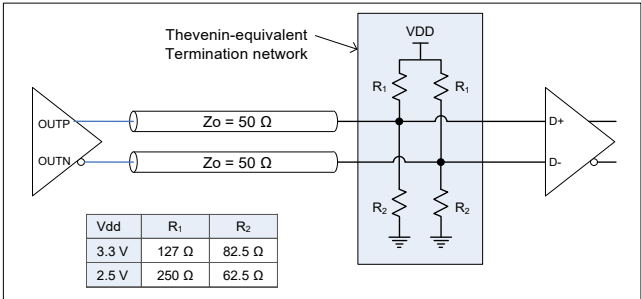


Figure 31. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network^[22]

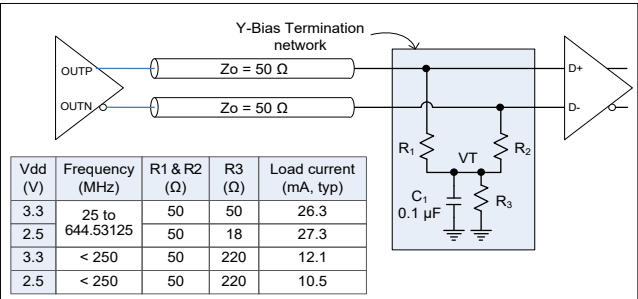


Figure 32. LVPECL and FlexSwing with Y-Bias Termination

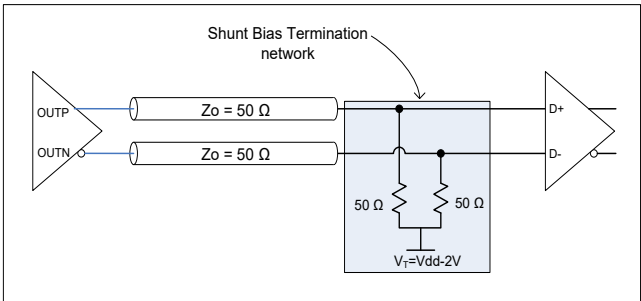


Figure 33. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

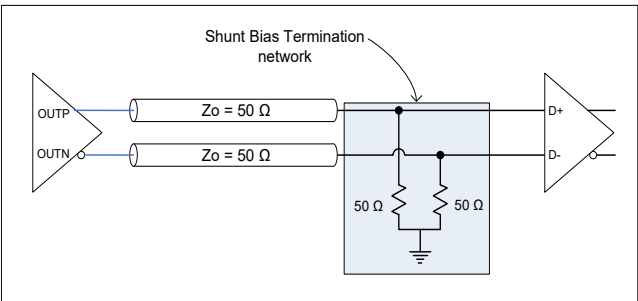


Figure 34. FlexSwing Termination – Only for use with Supply Voltage Order Code “18”

Termination Diagrams (continued)

LVDS, LVDS-2, LVDS-3, Supply Voltage: 1.8 V $\pm$ 5%, 2.5 V $\pm$ 10%, 3.3 V $\pm$ 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

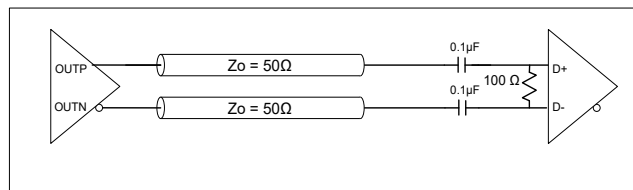


Figure 35. LVDS, LVDS-2, LVDS-3 AC Termination

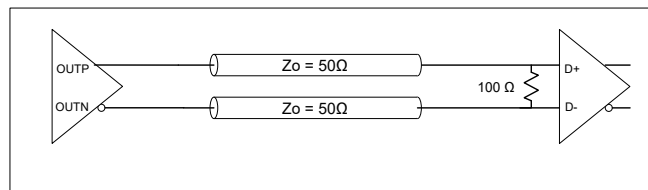


Figure 36. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V $\pm$ 5%, 2.5 V $\pm$ 10%, 3.3 V $\pm$ 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

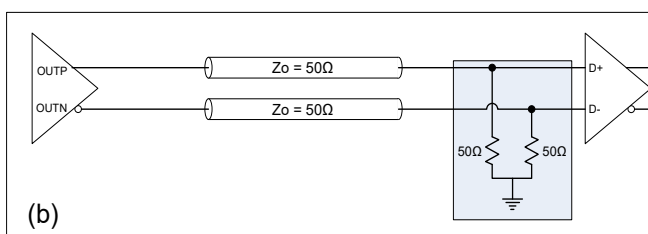
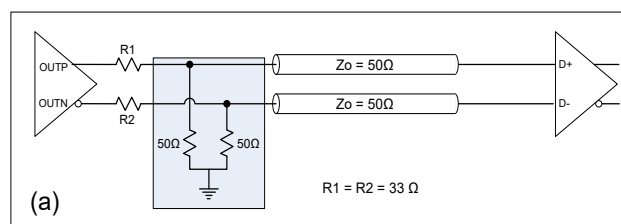


Figure 37. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V $\pm$ 5%, 2.5 V $\pm$ 10%, 3.3 V $\pm$ 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

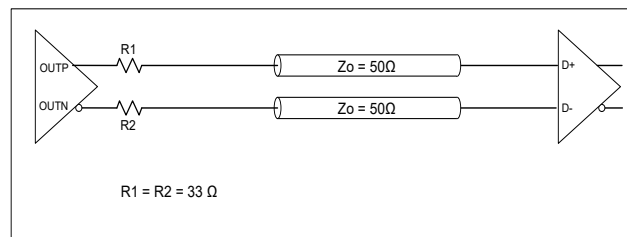
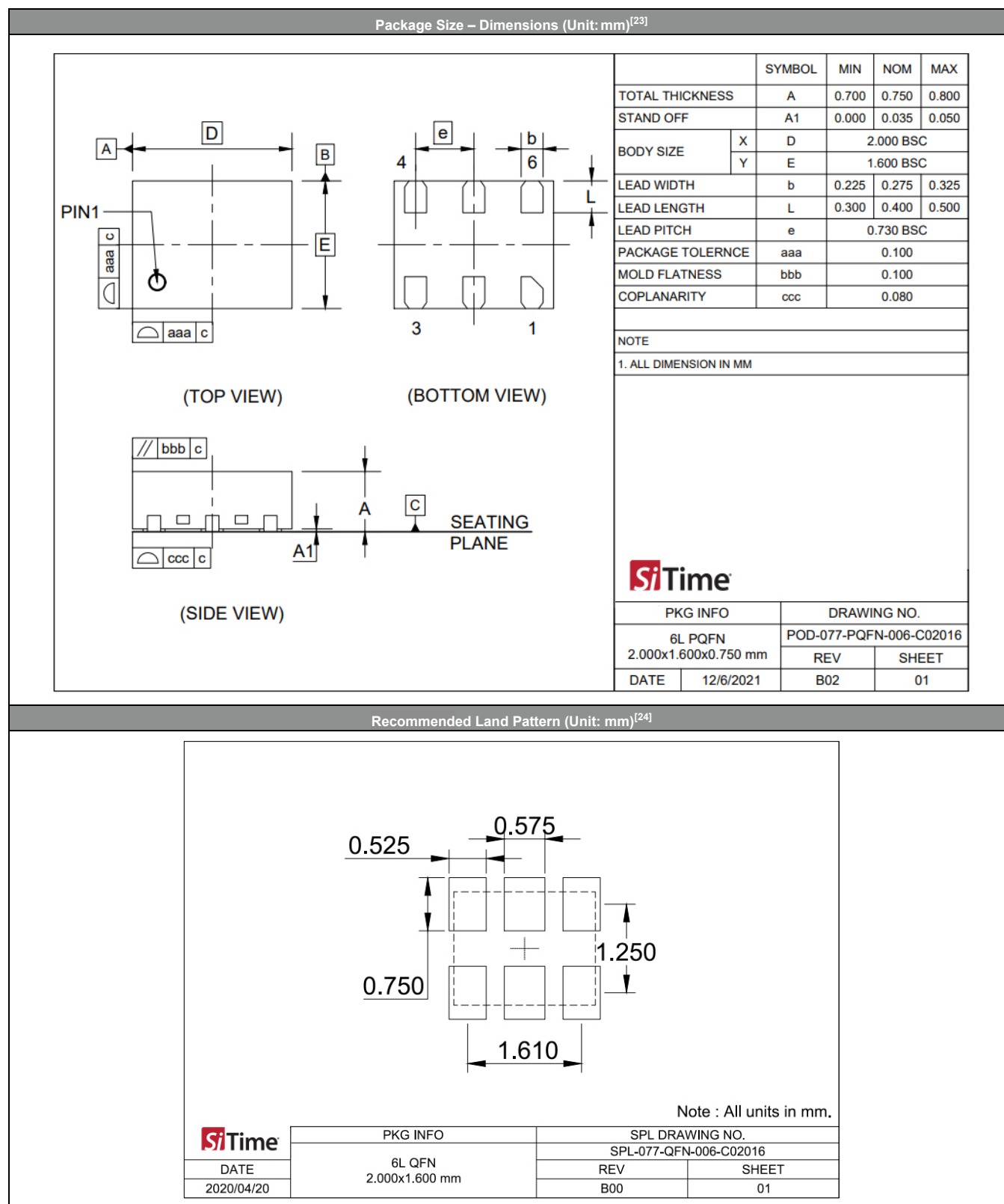


Figure 38. Low-power HCSL Termination

Notes:

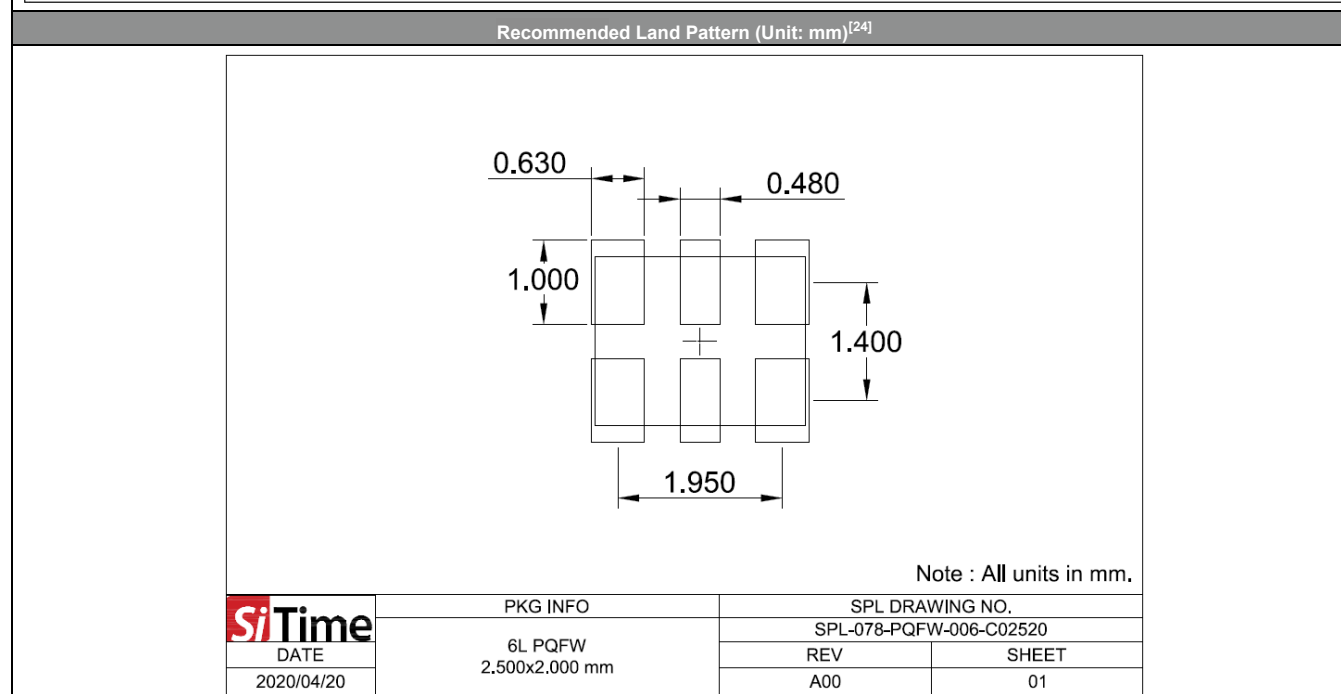
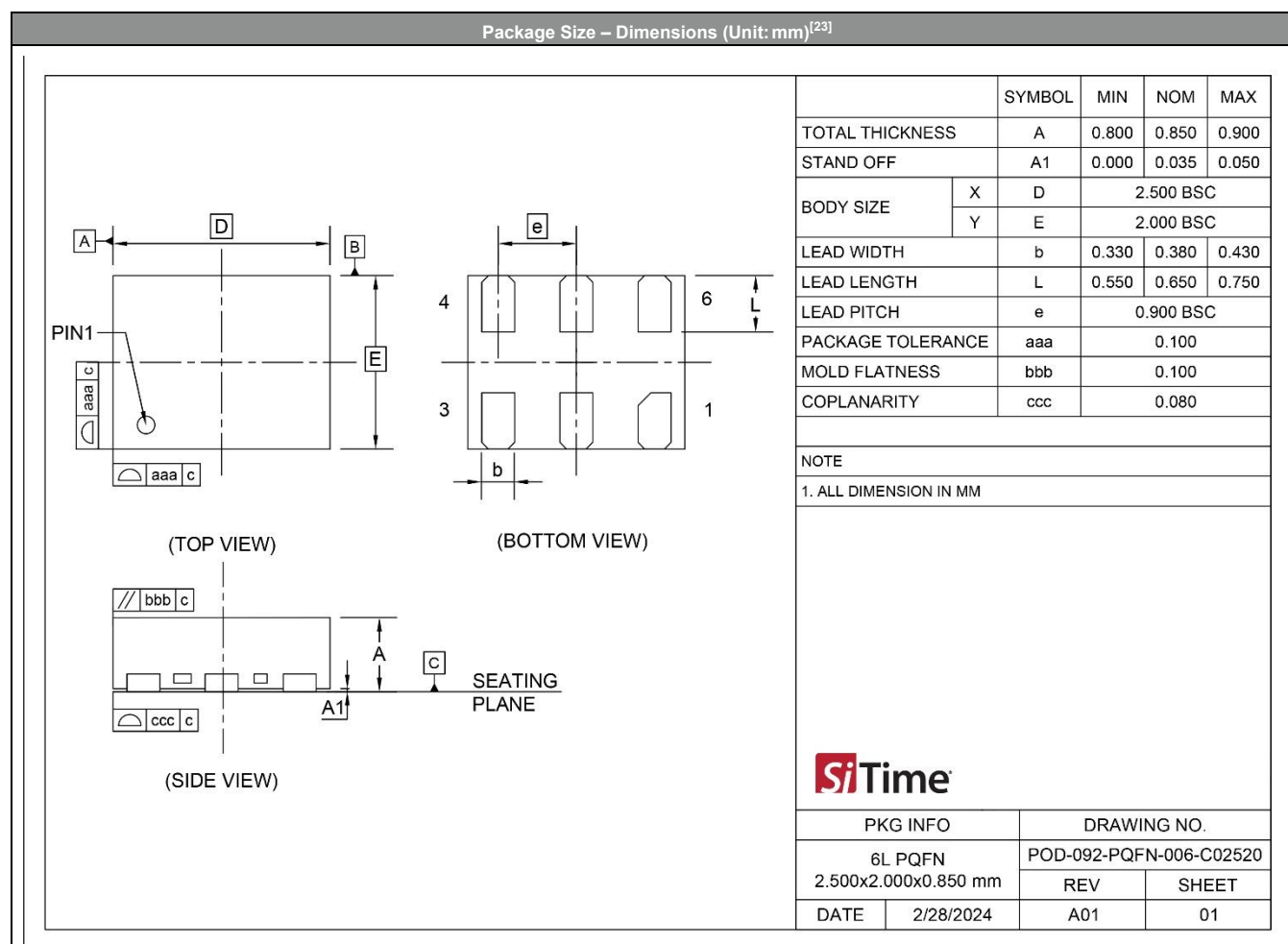
21. [Contact SiTime](#) for optimum R_B values for FlexSwing options.
22. [Contact SiTime](#) for optimum R_1 and R_2 values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

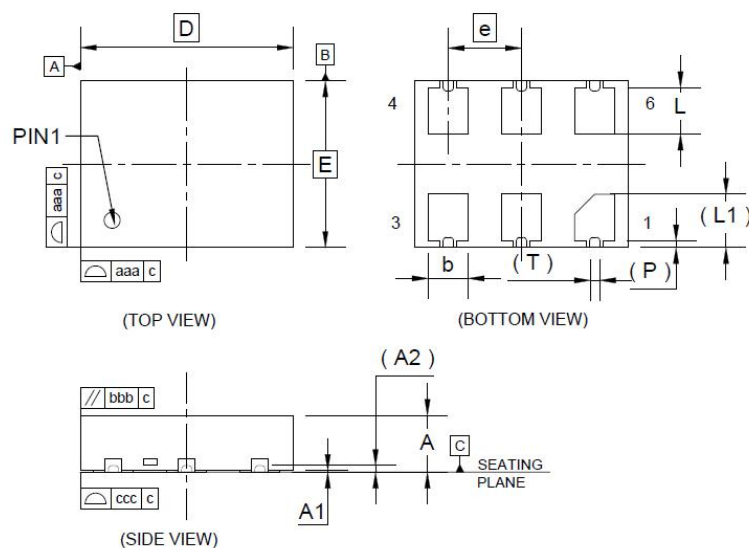


Notes:

23. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
24. A capacitor of value 0.1 μ F or higher between VDD and GND is required. An additional 10 μ F capacitor between VDD and GND is required for the best phase jitter performance.

Dimensions and Patterns — 2.5 x 2.0 mm x mm


Dimensions and Patterns — 3.2 x 2.5 mm x mm

Package Size – Dimensions (Unit: mm)^[23]

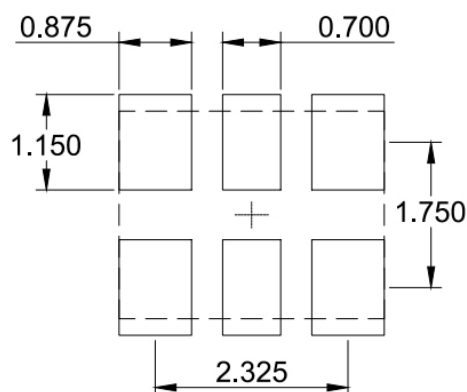
	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.800	0.850	0.900
STAND OFF	A1	0.000	0.035	0.050
BODY SIZE	X	D	3.200 BSC	
	Y	E	2.500 BSC	
LEAD WIDTH	b	0.550	0.600	0.650
LEAD LENGTH	L	0.650	0.700	0.750
	L1	0.800 REF		
LEAD PITCH	e	1.100 BSC		
PACKAGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	bbb	0.100		
COPLANARITY	ccc	0.080		
DIMPLE WIDTH	T	0.150 REF		
DIMPLE LENGTH	P	0.150 REF		
DIMPLE DEPTH	A2	0.100 REF		

NOTE

1. ALL DIMENSION IN MM



PKG INFO		DRAWING NO.	
6L PQFD 3.200x2.500x0.850 mm		POD-076-PQFD-006-C03225	
DATE	10/11/2022	REV	SHEET
		B01	01

Recommended Land Pattern (Unit: mm)^[24]

Note : All units in mm.

	PKG INFO	SPL DRAWING NO.	
	6L QFN 3.200x2.500 mm	SPL-076-QFN-006-C03225	
DATE		REV	SHEET
2020/04/20		B00	01

Additional Information

Table 22. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	https://www.sitime.com/support/resource-library/user-manuals/sit6760eb-evaluation-board-user-manual

Revision History

Table 23. Revision History

Revision	Release Date	Change Summary
1.0	1-Nov-2024	Updated 2520 package Dimensions drawing Rev 1.0 Production Release
1.1	13-May-2025	Added 50 MHz to the list of frequencies supported
1.2	22-Aug-2025	Added LVDS-2, LVDS-3 signaling support
1.3	16-Mar-2026	Added Phase Noise data for 156.25 MHz and 312.5 MHz in Table 3. And corresponding phase noise plots for 156.25 MHz (figure 4) & 312.5 MHz (figure 5)
1.31	30-Jul-2026	Updated symbol names from PSIJS to PSIJS and from PSIPN to PSIPN Updated disclaimer

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