# SiT92318

8 Output DB800Z Equivalent with 85/100 Ω Terminations

## Description

The SiT92318 family of parts are HCSL Low-Power (HCSL-LP), 8 output differential Fan-Out buffers that meet or exceed all the performance requirements of the Intel DB800Z specification. They are suitable for PCI-Express Gen1–7 or QP/UPI applications.

The SMBus interface and multiple output-enable pins allow the configuration and control of all 8 outputs individually.

It is packaged in a compact VQFN package and uses a standard pin configuration.

## Applications

- Micro server and tower server
- Rack server
- Storage area network (SAN) and host bus adapter (HBA) card
- Network attached storage (NAS)
- Hardware accelerator

## Features

- HCSL-LP outputs with Zo = 85 Ω or 100 Ω
- Saves power and board space – no termination resistors required
- Supports PCIe and QPI applications
- Spread spectrum compatible; tracks spreading input clock for low EMI
- Additive phase jitter
  - Fclk=156.25 MHz (12k-20M) band ~32 fs (Typical)
  - Fclk=100 MHz
    - PCIE Gen5 (CC) filter ~13 fs RMS
    - PCIE Gen6 filter (CC) ~8 fs RMS
    - PCIE Gen7 filter (CC) ~6 fs RMS
- Programmable output slew rate control
- 3.3 V core and IO supply voltages
- Hardware-controlled low power mode (PDN)
- Current consumption: 59.4 mA Typical with all 8 outputs enabled at 100 MHz, driving a 10 inch T line and 2 pF load on each output

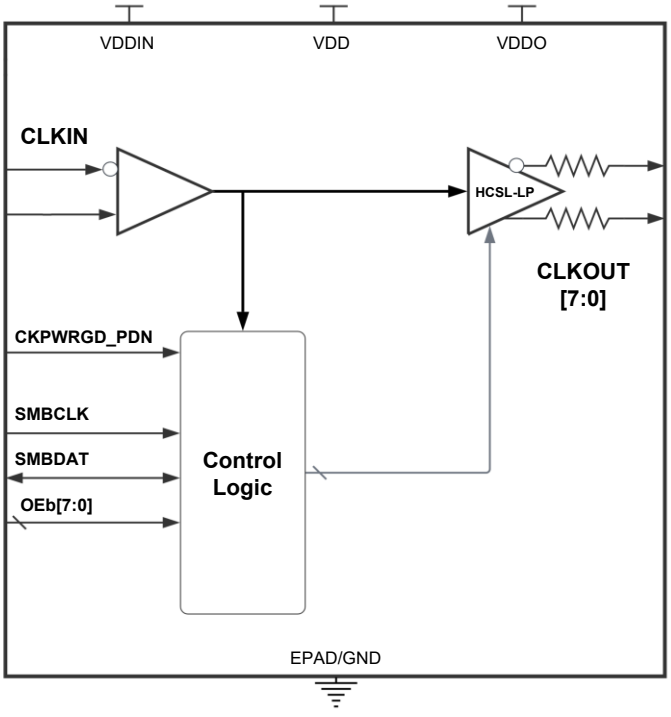


**Figure 1. SiT92318 Functional Overview**

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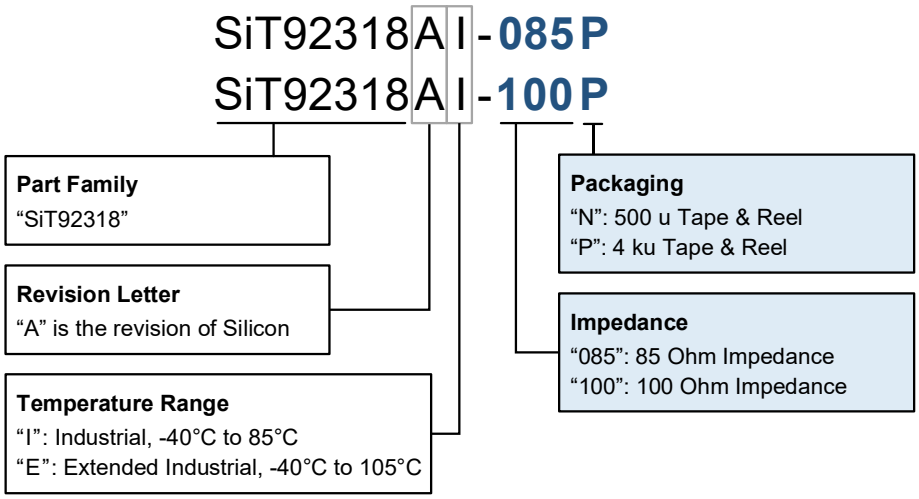
## Ordering Information



# Electrical Characteristics

## Table 1. Absolute Maximum Ratings

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Voltage** | Input Supply<br>Core Supply | VDDIN<br>VDD | | | 3.63 | V |
| **Output Bank Supply Voltage** | Output Driver Supply | VDDO | | | 3.63 | V |
| **Input Low Voltage** | | $V_{IL}$ | GND-0.5 | | | V |
| **Input High Voltage** | Except for SMBus interface | $V_{IH}$ | | | VDD+0.5 | V |
| **Input High Voltage** | SMBus clock and data pins | $V_{IHSMB}$ | | | 3.6 | V |
| **Storage Temperature** | | $T_S$ | -65 | | 150 | °C |
| **Junction Temperature** | | $T_J$ | | | 125 | °C |
| **ESD (Human Body Model)** | JESD22A-114 | $ESD_{HBM}$ | | | 2000 | V |
| **ESD (Charge Device Model)** | | $ESD_{CDM}$ | | | 500 | V |
| **Latch Up** | JEDEC JESD78D | LU | | | 100 | mA |
| **Moisture Sensitivity Level** | | MSL | | 3 | | |

**Notes:**

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

## Table 2. Recommended Operating Supply and Temperature

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Supply Voltage** | | VDDIN | 2.97 | 3.3 | 3.465 | V |
| **Core Supply Voltage** | | VDD | 2.97 | 3.3 | 3.465 | V |
| **Output Supply Voltage** | | VDDO | 2.97 | 3.3 | 3.465 | V |
| **Ambient Temperature** | Industrial (I) | $T_A$ | -40 | | 85 | °C |
| | Extended industrial (E) | | -40 | | 105 | °C |
| **Junction Temperature** | | $T_J$ | | | 125 | °C |

## Table 3. Electrical Characteristics

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Operating Supply Current, CKPWRGD High[1,2]** | Input Supply Current, No Clock | $IDD_{VDDIN\_STATIC}$ | | 7.3 | 9.5 | mA |
| | Input Supply Current, 100 MHz Clock | $IDD_{VDDIN\_DYN}$ | | 7.4 | 9.5 | mA |
| | Core Supply Current, No Clock | $IDD_{VDD\_STATIC}$ | | 5.7 | 9.5 | mA |
| | Core Supply Current, 100M Clock (Industrial (I)) | $IDD_{VDD\_DYN}$ | | 9.3 | 16 | mA |
| | (Extended industrial (E)) | | | 9.3 | 18 | mA |
| **Output Supply Current, CKPWRGD High[1]** | Output Supply Current, No Clock | $IDD_{VDDO\_STATIC}$ | | 6.6 | 8 | mA |
| | All Outputs Enabled, driving a 10in T-line terminated with 2 pF cap at 100 MHz clock, SiT92318AIP | $IDD_{VDDO\_DYN}$ | | 59 | 93 | mA |
| | SiT92318AI100P | | | 54 | 84 | |
| **Power Down Current[1,2]** | CKPWRGD = Low | $IDD_{VDDIN\_PDN}$ | | 0.023 | 0.1 | mA |
| | | $IDD_{VDD\_PDN}$ | | 3.5 | 5 | mA |
| | | $IDD_{VDDO\_PDN}$ | | 0.44 | 1.25 | mA |
| **Input Control Pin Characteristics** | | | | | | |
| **Input high voltage – Logic inputs[2]** | | $V_{IH}$ | 0.7 x VDD | | | V |
| **Input low voltage – Logic inputs[2]** | | $V_{IL}$ | | | 0.3 x VDD | V |
| **Pin Inductance[3]** | | $L_{PIN}$ | | | 2 | nH |

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Capacitance[3]** | Logic Inputs, except DIF_IN. | $C_{IN}$ | | | 4.5 | pF |
| | DIF_IN differential clock inputs | $C_{INDIF\_IN}$ | | | 2.7 | |
| | Output pin capacitance | $C_{OUT}$ | | | 4.5 | |

**Notes:**
1. Guaranteed by characterization.
2. Guaranteed by production testing.
3. Guaranteed by design.

## Table 4. Input Clock Characteristics

Unless otherwise specified: VDDIN = 3.3 V ±5%, VDDO = 3.3 V ±5%, -40°C ≤ $T_A$ ≤ 105°C, CLKin driven differentially.

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input frequency range[1,2]** | | FCLKin | 1 | | 400M | Hz |
| **Peak differential input voltage swing[2]** | | VID | 0.1 | | | V |
| **Input Slew Rate - CLKIN[1]** | Measured differentially | dv/dt | 2 | | | V/ns |
| **Input Duty Cycle[1]** | Measurement from differential waveform | dTIN | | 50 | | % |
| **Input Crossover Voltage[2]** | Crossover voltage | | 0.1 | | 0.9 | V |

**Notes:**
1. All parameters are guaranteed by Characterization.
2. Guaranteed by production testing.

## Table 5. Output Clock Characteristics (HCSL-LP) at 100 MHz

$T_A = T_{COM}$; Supply Voltage VDDO = 3.3 V ±5%

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Slew rate[1][5][6]** | Scope averaging on | Trf | 2.4 | 2.9 | 3.5 | V/ns |
| **Slew rate matching[1]** | Slew rate matching, Scope averaging on | ΔTrf | | | 18 | % |
| **Voltage High[1][5][6]** | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) (Industrial (I)) | $V_{High}$ | 721 | 794 | 868 | mV |
| | (Extended industrial (E)) | $V_{High}$ | 721 | 794 | 870 | mV |
| **Voltage Low[1][5]** | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | $V_{Low}$ | -86 | 11 | 84 | mV |
| **Max Voltage[1][5][6]** | Measurement on single ended signal using absolute value. (Scope averaging off) (Industrial (I)) | $V_{max}$ | 811 | 856 | 890 | mV |
| **Min Voltage[1][5]** | | $V_{min}$ | -119 | -49 | 22 | |
| | (Extended industrial (E)) | $V_{min}$ | -119 | -49 | 32 | |
| **Vswing[1][5][6]** | Scope averaging off [pk to pk, single ended] | $V_{SWING}$ | 841 | 905 | 973 | mV |
| **Crossing Voltage (abs)[1]** | Scope averaging off | Vcross_abs | 380 | 423 | 455 | mV |
| **Crossing Voltage (var)[1]** | Scope averaging off | Δ-Vcross | -19 | 27 | 71 | mV |
| **Differential Impedance[2]** | SiT92318AIP | $Z_{DIFF}$ | 80 | 85 | 90 | Ω |
| | SiT92318AI100P | | 94 | 100 | 106 | Ω |
| **Clock Stabilization[3,4]** | From VDDO power-up and after input clock stabilization or assertion of CKPWRGD to 1st Clock | $T_{STAB}$ | | 1.0 | 1.8 | ms |
| **OEb Latency[3,4]** | DIF starts after OEb assertion DIF stop after OEb de-assertion | $t_{LATOEb}$ | 4 | | 6 | Clocks |
| **Tdrive_PDb[3,4]** | DIF output enable after CKPWRGD assertion | $t_{DRVPDb}$ | | 100 | 300 | µs |

**Notes:**
1. Guaranteed by characterization,measured on 10 inch T-line with 2pf load.
2. Guaranteed by production testing.
3. Control input must be monotonic from 20% to 80% of input swing.
4. Guaranteed by limited testing of typical parts.

5. Default factory configuration.
6. The cpk = 1.33.

## Table 6. SMBUS Electrical Parameters

$T_A = T_{AMB}$. Supply voltages are per normal conditions. See Test loads for loading conditions.

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SMBus Input Low Voltage[1]** | | $V_{ILSMB}$ | | | 0.3 x VDD | V |
| **SMBus Input High Voltage[1]** | | $V_{IHSMB}$ | 0.7 x VDD | | VDD | V |
| **Hysteresis on SMBUS pins** | | $V_{HYS}$ | 0.048 | | | V |
| **SMBus Output Voltage[1]** | $I_{OH}$ = -2 mA | $V_{OHSMB}$ | 0.75 x VDD | | | V |
| | $I_{OL}$ = 2 mA | $V_{OLSMB}$ | | | 0.25 x VDD | V |
| **SMBus Operating Frequency[1]** | | $f_{SMB}$ | 4 | | 400 | kHz |
| **Max Capacitive Load for Each Bus line** | | $C_B$ | | 400 | | pf |

**Notes:**

1. Guaranteed by characterization.

## Table 7. Skew and Differential Jitter Parameters

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CLK INx, CLKOUTx[1,2,4,5,6,7,9]** | Input-to-Output Skew in nominal value @ 25°C, 3.3 V (Industrial (I)) | $t_{PD}$ | 455 | 600 | 723 | ps |
| | (Extended industrial (E)) | $t_{PD}$ | 411 | 600 | 744 | ps |
| **CLKINx, CLKOUTx[1,2,6,7,8]** | Input-to-Output Skew Variation across temperature | $T_{PD\_DRIFT}$ | | 0.4 | 0.82 | ps/C |
| **DIF[1,2,5,6,7,9]** | Output-to-Output Skew across all outputs (Industrial (I)) | $t_{SKEW\_ALL}$ | | | 50 | ps |
| | (Extended industrial (E)) | $t_{SKEW\_ALL}$ | | | 50 | ps |
| **DIF Skew** | Ouptut to output skew variation across temp | | | | 0.07 | ps/C |
| **Duty Cycle Distortion[1,3,5,6]** | Measured differentially, @100MHz | $t_{DCD}$ | -1 | 0.1 | 1 | % |

**Notes:**

1. Guaranteed by characterization.
2. Differential cross-point to differential cross-point measurement.
3. The difference in Duty Cycle between the output and input clock is referred as Duty Cycle Distortion.
4. Mean Value measured through scope averaging.
5. Measured from differential waveform.
6. Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
7. All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
8. This is the amount of input-to-output delay variation with respect to temperature.
9. The cpk = 1.33.

## Table 8. PCIe Phase Jitter Parameters with 100 MHz Clock

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Additive Phase Jitter Common Clock** | PCIe Gen 1 HF[1,2,3,4] | $tjph_{PCIeG1-CC}$ | | 1.9 | 4.7 | ps (p-p) |
| | PCIe Gen 2 HF[1,2,3,4,5,6] | $tjph_{PCIeG2-CC}$ | | 102 | 138.4 | fs rms |
| | PCIe Gen 2 LF[1,2,3,4,5,6] | $tjph_{PCIeG2-CC}$ | | 4 | 7.7 | fs rms |
| | PCIe Gen 3[1,2,3,4,5,6] | $tjph_{PCIeG3-CC}$ | | 33 | 44.3 | fs rms |
| | PCIe Gen4[1,2,3,4,5,6] | $tjph_{PCIeG4-CC}$ | | 33 | 44.3 | fs rms |
| | PCIe Gen5[1,2,3,4,5,6] | $tjph_{PCIeG5-CC}$ | | 13 | 17.5 | fs rms |
| | PCIe Gen6[1,2,3,4,5,6] | $tjph_{PCIeG6-CC}$ | | 8 | 10.6 | fs rms |
| | PCIe Gen7[1,2,3,4,5,6] | $tjph_{PCIeG7-CC}$ | | 5 | 7.4 | fs rms |
| **Additive Phase Jitter SRIS** | PCIe Gen 2 HF[1,2,3,45,6] | $tjph_{PCIeG2-SRIS}$ | | 70 | 122.7 | fs rms |
| | PCIe Gen 2 LF[1,2,3,4,5,6] | $tjph_{PCIeG2-SRIS}$ | | 18 | 2.8 | fs rms |
| | PCIe Gen 3[1,2,3,4,5,6] | $tjph_{PCIeG3-SRIS}$ | | 29 | 53.7 | fs rms |
| | PCIe Gen4[1,2,3,4,5,6] | $tjph_{PCIeG4-SRIS}$ | | 30 | 55.3 | fs rms |
| | PCIe Gen5[1,2,3,4,5,6] | $tjph_{PCIeG5-SRIS}$ | | 10 | 17.1 | fs rms |
| | PCIe Gen6[1,2,3,4,5,6] | $tjph_{PCIeG6-SRIS}$ | | 7 | 11.0 | fs rms |
| | PCIe Gen7[1,2,3,4,5,6] | $tjph_{PCIeG7-SRIS}$ | | 4 | 8.7 | fs rms |
| **Additive Phase Jitter SRNS** | PCIe Gen 2 HF[1,2,3,4,5,6] | $tjph_{PCIeG2-SRNS}$ | | 68 | 110.2 | fs rms |
| | PCIe Gen 2 LF[1,2,3,4,5,6] | $tjph_{PCIeG2-SRNS}$ | | 1 | 1.3 | fs rms |
| | PCIe Gen 3[1,2,3,4,5,6] | $tjph_{PCIeG3-SRNS}$ | | 24 | 36.2 | fs rms |

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | PCIe Gen4[1,2,3,4,5,6] | $tjph_{PCIeG4-SRNS}$ | | 24 | 36.2 | fs rms |
| | PCIe Gen5[1,2,3,4,5,6] | $tjph_{PCIeG5-SRNS}$ | | 9 | 13.2 | fs rms |
| | PCIe Gen6[1,2,3,4,5,6] | $tjph_{PCIeG6-SRNS}$ | | 6 | 9.7 | fs rms |
| | PCIe Gen7[1,2,3,4,5,6] | $tjph_{PCIeG7-SRNS}$ | | 4 | 6.8 | fs rms |

**Notes:**

1. Guaranteed by design and characterization. Applies to all differential outputs.
2. Input to SIT92318 is fed using low phase noise source SMA100B while SIT92318 is configured as 100 MHz LP-HCSL Output Driver and fed to the channels of the DSO through low noise high slew drivers to minimize the impact of DSO broadband noise.
3. Additive RMS Jitter Measurement for PCIe are made using DSO. Commercially available and popular PCIe jitter post processing tools are used to report PCIe jitter.
4. Additive jitter for RMS values is calculated by solving the equation for b [ $b = \sqrt{(c^2 - a^2)}$ ] where 'a' is the rms input jitter and "c" is the rms total jitter.
5. Input to SIT92318 is fed using low phase noise source SMA100B, SIT92318 is configured as 100MHz HCSL Output Driver [VDDOx = 3.3 V] and fed to the channels of DSA90804A using the exact measurement set up.
6. For each type of PCIE jitter – Common Clock, SRIS, SRNS, there are 64 possible PCIE GEN filter values. We take the worst case jitter value over process, voltage and temperature among these 64 filters. The spec of H1, H2 (TX, RX PLL transfer functions) are F3dB = [2,4,5] MHz, Peaking = [0.01, 1, 2] dB, For H3 filter F3dB=[10] MHz.

## Table 9. Phase Jitter Parameters

| Parameters | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Additive Phase Jitter** | Fclk = 156.25M, 12K-20MHz (Industrial (I)) | tjph_12K_20M | | 32 | 42.0 | fs rms |
| | Fclk = 156.25M, 12K-20MHz (Extended Industrial (E)) | | | | 44.0 | |
| | Fin = 312.5 MHz 12K-20MHz with 4MHz HPF[1] (Industrial (I)) | tjph_420B | | 20 | 28.5 | fs rms |
| | Fin = 312.5 MHz 12K-20MHz with 4MHz HPF[1] (Extended Industrial (E)) | | | | 30.0 | |

**Notes:**

1. HPF: High Pass Filter.

## Pin Configuration

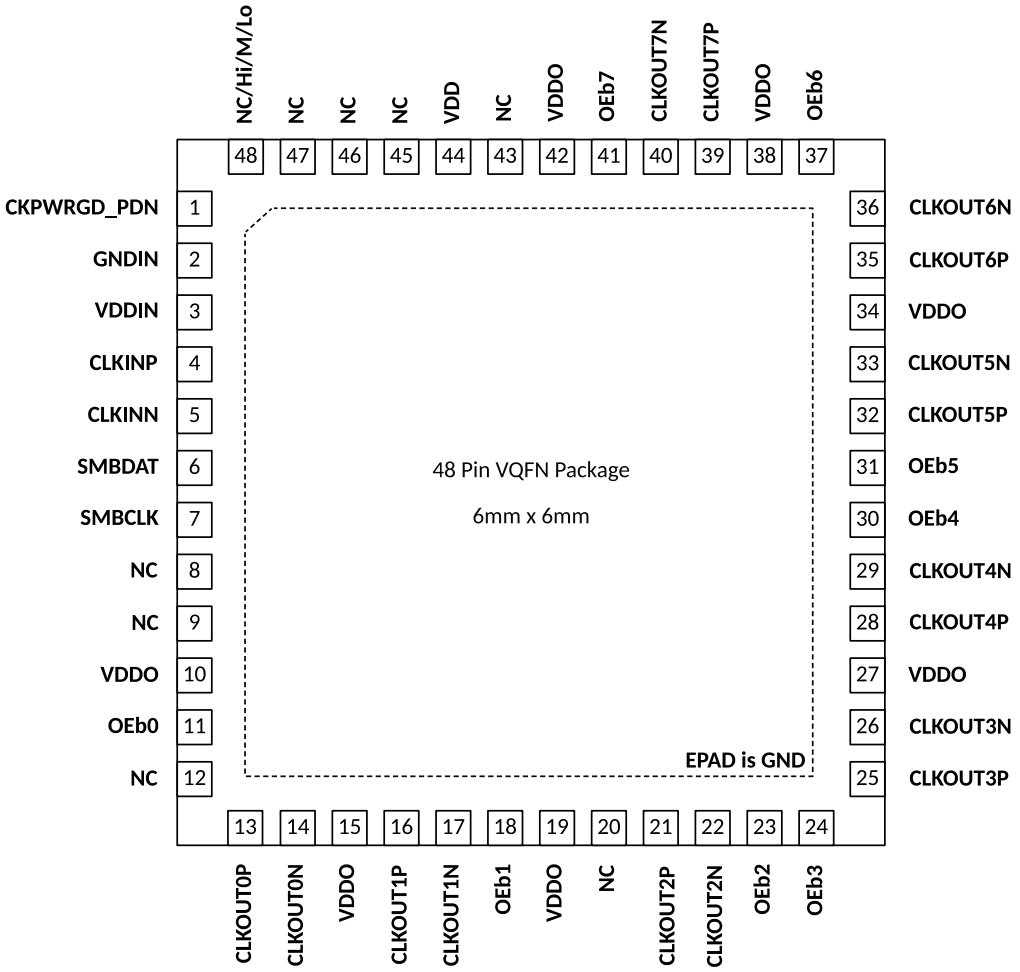



**Figure 2. Pin Configuration**

### Table 10. Pin Description

| Pin Name | Pin No. | I/O Type | Description |
|---|---|---|---|
| CKPWRGD_PDN | 1 | I,PU,PDT | 3.3 V Input notifies device to sample latched inputs and start up on first high assertion or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| GNDIN | 2 | Ground | Differential Input clock (receiver) GND |
| VDDIN | 3 | PWR | 3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| CLKINP | 4 | I,PDT | 0.8 V Differential True input |
| CLKINN | 5 | I,PDT | 0.8 V Differential Complementary Input |
| SMBDAT | 6 | I/O, OD, PDT | Data pin of SMBUS circuitry, 3.3 V tolerant . Recommend to connect external 3.3Kohm pull up resistor for SMBUS operation. |
| SMBCLK | 7 | I, OD, PDT | Clock pin of SMBUS circuitry, 3.3 V tolerant. Recommend to connect external 3.3Kohm pull up resistor for SMBUS operation. |
| NC/Hi/M/Lo | 48 | N/A | This pin does not have any specific user function. NC or any static level will be acceptable. |
| NC | 8, 9, 12, 20,43,45, 46,47 | N/A | No Connection. Recommended to be grounded. |
| VDDO | 10, 15, 19, 27, 34, 38, 42 | PWR | Power Supply for the Output Drivers, nominal 3.3 V |

| Pin Name | Pin No. | I/O Type | Description |
|---|---|---|---|
| OEb0 | 11 | I, PD, PDT | Active low input for enabling Clock pair 0.<br>1 = disable outputs,<br>0 = enable outputs |
| CLKOUT0P | 13 | O | 0.85 V differential true clock output |
| CLKOUT0N | 14 | O | 0.8 V differential Complementary clock output |
| CLKOUT1P | 16 | O | 0.8 V differential true clock output |
| CLKOUT1N | 17 | O | 0.8 V differential Complementary clock output |
| OEb1 | 18 | I, PD, PDT | Active low input for enabling Clock pair 1.<br>1 = disable outputs,<br>0 = enable outputs |
| CLKOUT2P | 21 | O | 0.8 V differential true clock output |
| CLKOUT2N | 22 | O | 0.8 V differential Complementary clock output |
| OEb2 | 23 | I, PD, PDT | Active low input for enabling Clock pair 2.<br>1 = disable outputs,<br>0 = enable outputs |
| OEb3 | 24 | I, PD, PDT | Active low input for enabling Clock pair 3.<br>1 = disable outputs,<br>0 = enable outputs |
| CLKOUT3P | 25 | O | 0.8 V differential true clock output |
| CLKOUT3N | 26 | O | 0.8 V differential Complementary clock output |
| CLKOUT4P | 28 | O | 0.8 V differential true clock output |
| CLKOUT4N | 29 | O | 0.8 V differential Complementary clock output |
| OEb4 | 30 | I, PD, PDT | Active low input for enabling Clock pair 4.<br>1 = disable outputs,<br>0 = enable outputs |
| OEb5 | 31 | I, PD, PDT | Active low input for enabling Clock pair 5.<br>1 = disable outputs,<br>0 = enable outputs |
| CLKOUT5P | 32 | O | 0.8 V differential true clock output |
| CLKOUT5N | 33 | O | 0.8 V differential Complementary clock output |
| CLKOUT6P | 35 | O | 0.8 V differential true clock output |
| CLKOUT6N | 36 | O | 0.8 V differential Complementary clock output |
| OEb6 | 37 | I, PD, PDT | Active low input for enabling Clock pair 6.<br>1 = disable outputs,<br>0 = enable outputs |
| CLKOUT7P | 39 | O | 0.8 V differential true clock output |
| CLKOUT7N | 40 | O | 0.8 V differential Complementary clock output |
| OEb7 | 41 | I, PD, PDT | Active low input for enabling Clock pair 7.<br>1 = disable outputs,<br>0 = enable outputs |
| VDD | 44 | PWR | 3.3 V power for the Core Supply. |

**Note:**

1 PU is weak internal Pull-up with 200 KΩ resistor.
2 PD is weak internal Pull-down with 200 KΩ resistor.
3 PDT (Power Down Tolerant) pins can be driven when the device is powered down without accidentally waking up the device.
4 Clock input pins are power down tolerant for voltage level < 1.8V on pins.
5 OD (Open Drain). It requires an external Pull-up on the board.
6 'b' suffix (in OEb) indicates an active-low control.

# Functional Description

## Typical Application

Figure 3 shows a SIT92318 typical application. In this application, a clock generator provides a 100-MHz reference to the SIT92318 which then distributes that clock to PCIe endpoints.

The clock generator may either be a discrete clock generator, or it may be integrated in a larger component such as a Platform Controller Hub (PCH) or application processor.

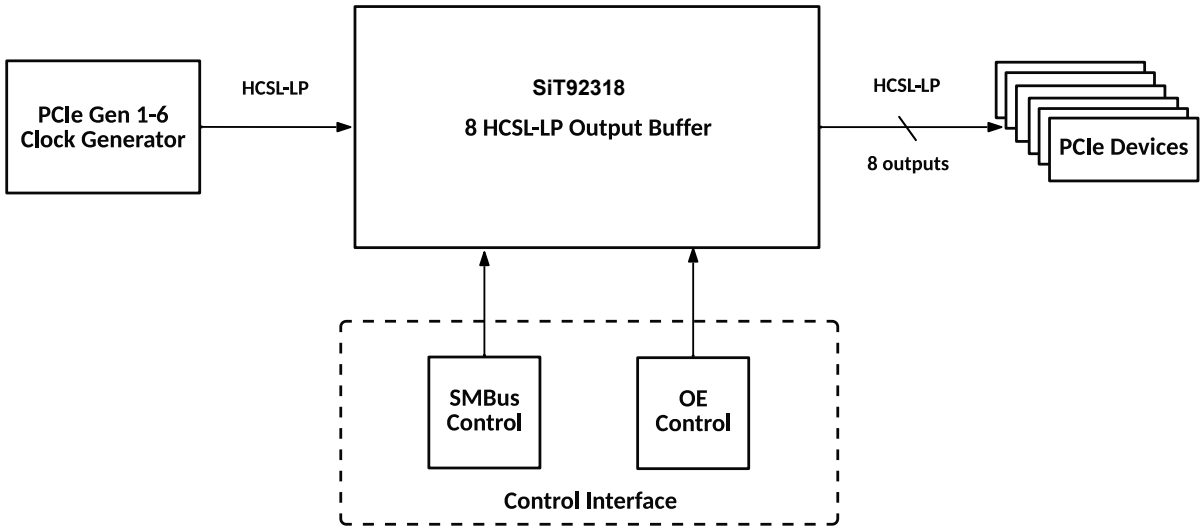



**Figure 3. Typical Application Diagram**

## Parameter Measurement Information

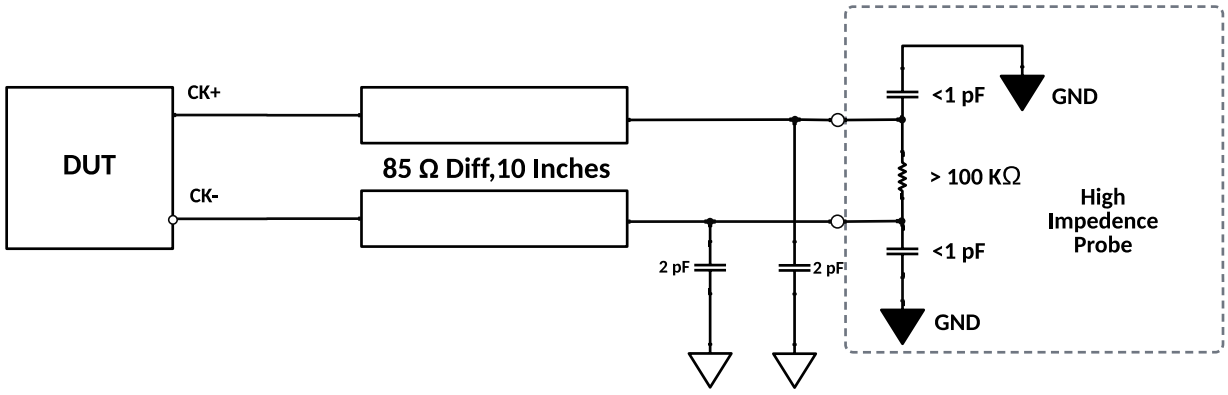



**Figure 4. AC Test Mode**

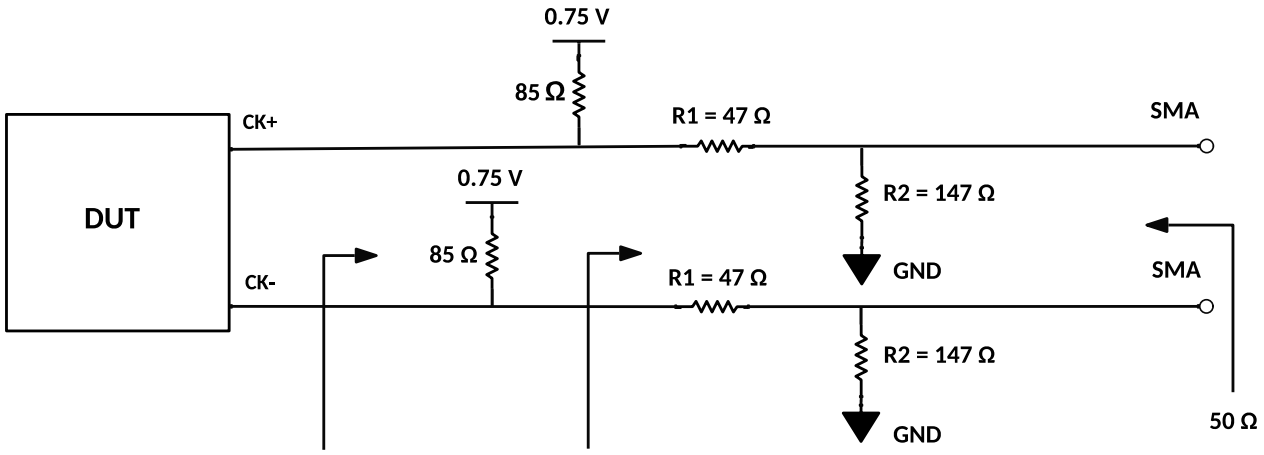



**Figure 5. DC Simulation Mode**

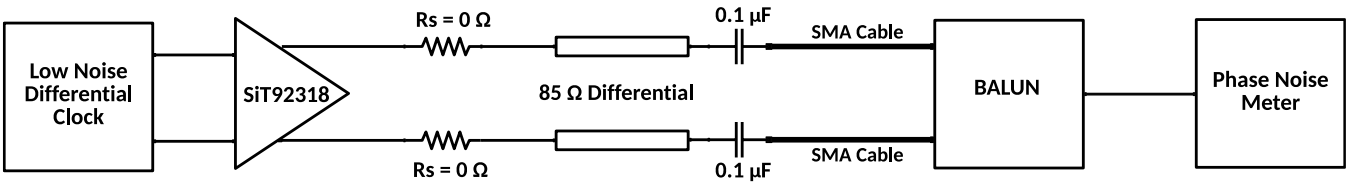



**Figure 6. Phase Noise Measurement Setup**

### Table 11. Input vs Output States

| Control Inputs | CLKIN | OEb[7:0] HARDWARE PINS AND SMBus CONTROL REGISTER BIT | | | CLKOUT[7:0]_P / CLKOUT[7:0]_N |
|---|---|---|---|---|---|
| CKPWRGD_PDN | | OE[7:0]b Pin | OUT_EN_CLK[7:0] | STOP_STATE_CONFIG_REG | |
| 1 | X | X | 0 | 0 | LOW/LOW |
| | | | | 1 | HiZ/HiZ |
| | | | | 2 | High/Low |
| | | | | 3 | Low/High |
| | | 1 | X | 0 | LOW/LOW |
| | | | | 1 | HiZ/HiZ |
| | | | | 2 | High/Low |
| | | | | 3 | Low/High |
| | Running | 0 | 1 | X | Output Follow input |
| 0 | X | X | X | 0 | LOW/LOW |
| | | | | 1 | HiZ/HiZ |
| | | | | 2 | High/Low |
| | | | | 3 | Low/High |

### Power Good Assertion and De-assertion

Power Good (CKPWRGD_PDN) is asserted high and de-asserted low. De-assertion of CKPWRGD_PDN (pulling the signal low) is equivalent to indicating a powerdown condition. CKPWRGD_PDN (assertion) is used by the DB800Z to sample initial configurations such as SA selections.

After CKPWRGD_PDN has been asserted high for the first time, the pin becomes a PWRDNb (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDNb is a completely asynchronous active low input.

When entering power savings mode, PWRDNb should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner.

When PWRDNb is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

**NOTE:** The assertion and de-assertion of PWRDNb is asynchronous.

**Warning:** Disabling of the CLKIN input clock prior to the assertion of PWRDNb is an undefined mode and is not recommended. Operation in this mode may result in glitches.

### Power Good De-Assertion

When PWRDNb is sampled low by two consecutive rising edges of CLKINN, all differential outputs must be held Tri-stated on the next CLKINN high to low transition.

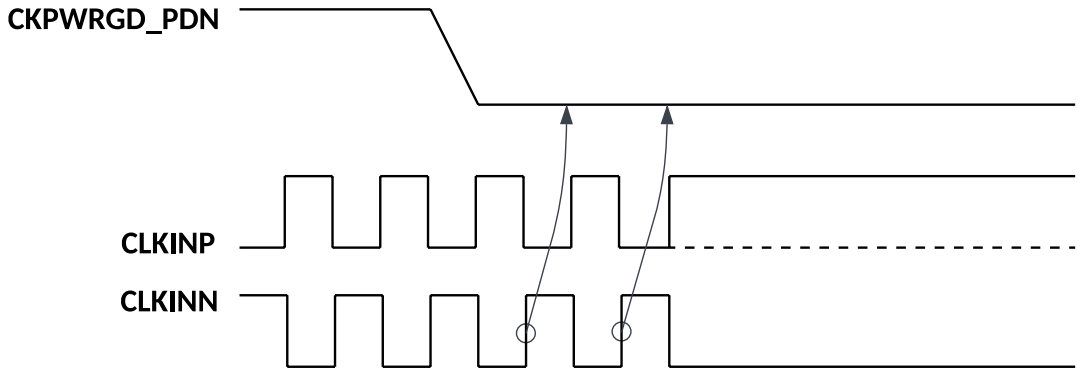



**Figure 7. Power Good Assertion**

### Power Good Assertion

CKPWRGD_PDN must not be asserted to the clock buffer before VDD reaches $VDD_{MIN}$. Prior to $VDD_{MIN}$ it is recommended to hold PWRGD low (less than 0.5 V).

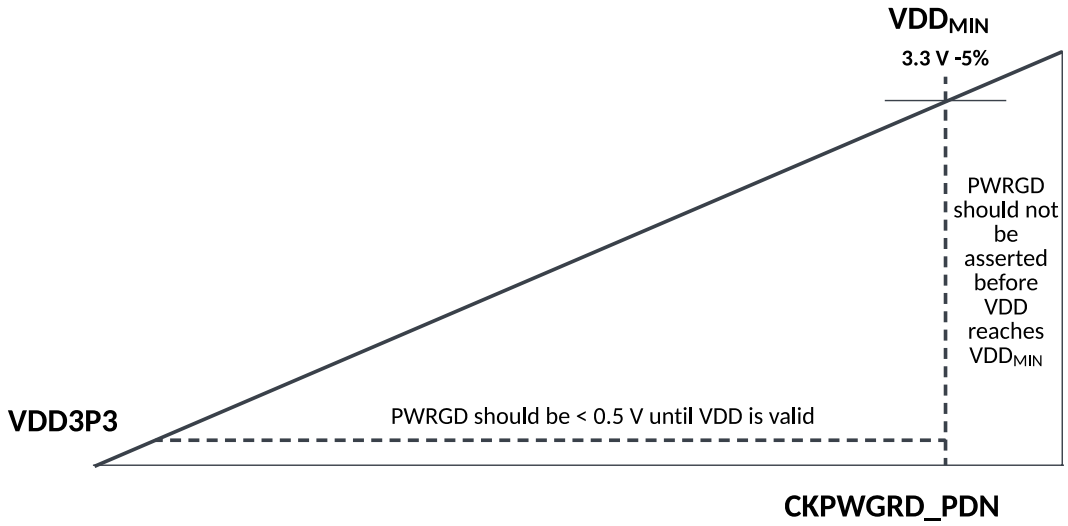



**Figure 8. Power Good vs VDD3P3 relationship**

The power-up latency in $T_{STABLE}$ is to be less than 1.8 ms. This is the time from the valid CLKINx input and the assertion of the PWRGD signal until the output of the stable clocks from the buffer chip.

All differential outputs stopped in a Tri-state condition resulting from power down must be driven high in less than 300 µs of the PWRGD assertion to a voltage greater than 200 mV.

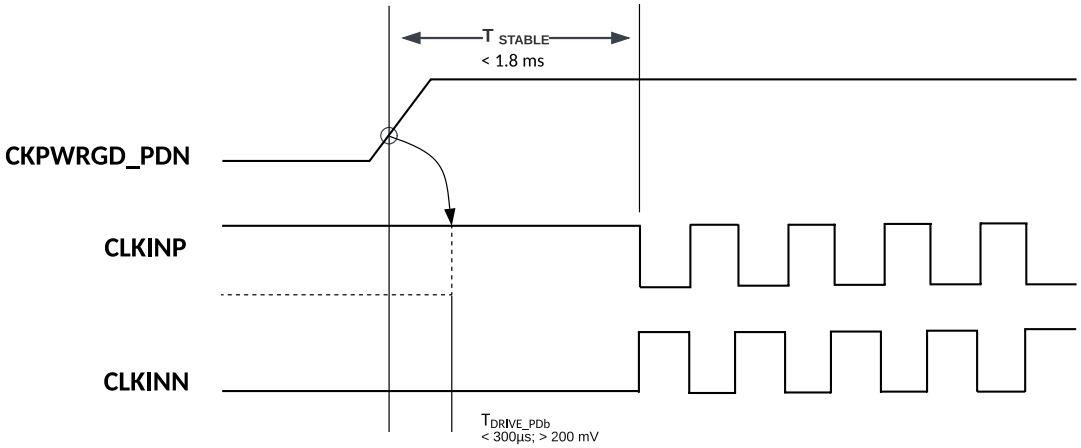



**Figure 9. Power Good Assertion**

## Serial Interface Information: SMBus

System Management Bus (SMBus) is a 2 wire interface, which uses SMBCLK and SMBDAT on the device for serial communication. SMBus will be active only when CKPWRGD_PDN is High ($V_{IH}$).

### Generic SMBus Description

The Figure 10 illustrates a generic SMBus sequence along with the description and functions of the constituent bytes elaborated in Table 12.

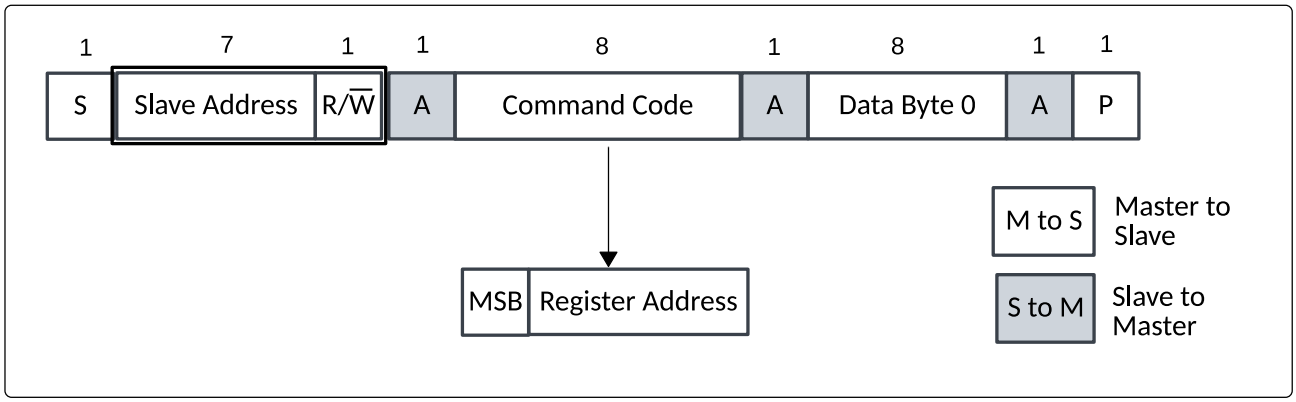



**Figure 10. Generic SMBus Sequence**

**Table 12. SMBus Address Register Description**

| Description | Bit Range | Function |
|---|---|---|
| S | 1 | Start Condition |
| Sr | 1 | Repeated start condition |
| Slave Address | 7 [7:1] | Address of the slave device. |
| R/$\overline{W}$ | 1 [LSB] | 1 = Read (Rd), 0 = Write (Wr) |
| A | 1 | 1 = No-Acknowledgement (NA), 0 = Acknowledgement (A) |
| P | 1 | Stop condition |
| Command Code | 1 [MSB] | 1 = Byte read/write, 0 = Block read/write |
| | 7 [6:0] | Register address |

The register number should be specified when reading or writing a register in a SMBus slave device. While mentioning the register address, MSB must be SET for byte operation and must be RESET for block operations.

## SMBus Byte: Read and Write Operations

### Byte Read

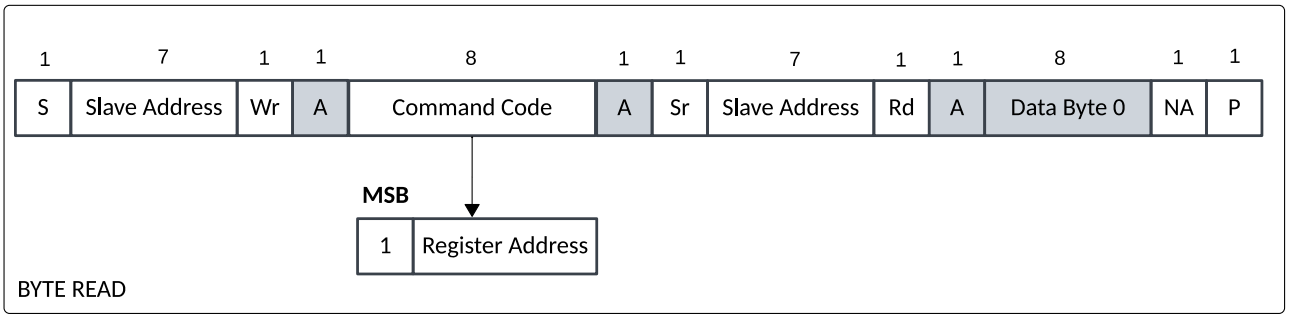



**Figure 11. Byte Read Operation**

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 1 and byte read starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends a repeated start bit
- Master sends the slave address with LSB = Read
- Slave device will send acknowledgement (A)
- Slave device will send data byte
- Master will send not-acknowledgment (NA)
- Master will send a stop bit

### Byte Write

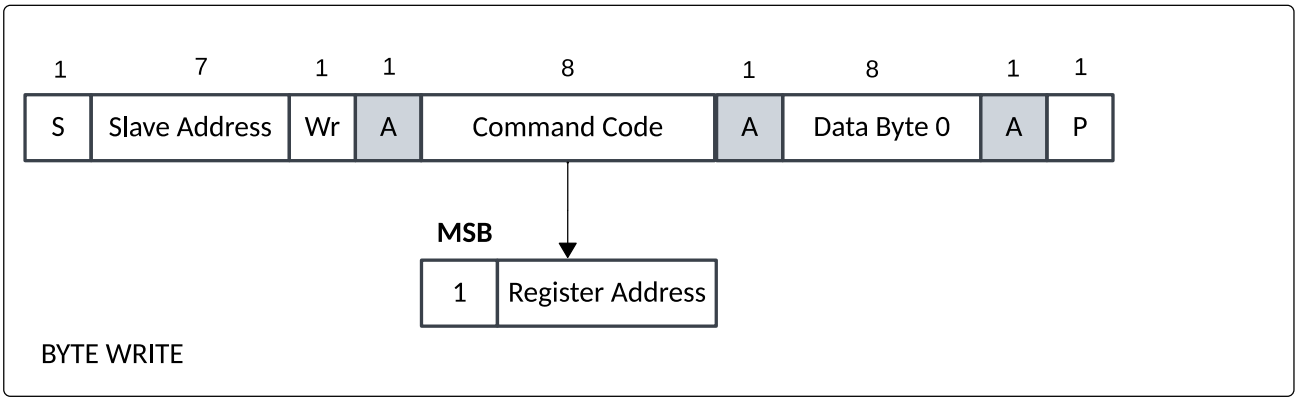



**Figure 12. Byte Write Operation**

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 1 and byte write starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends data byte to be written
- Slave device will send acknowledgement (A)
- Master sends a stop bit

## SMBus Block: Read and Write Operations

### Block Read

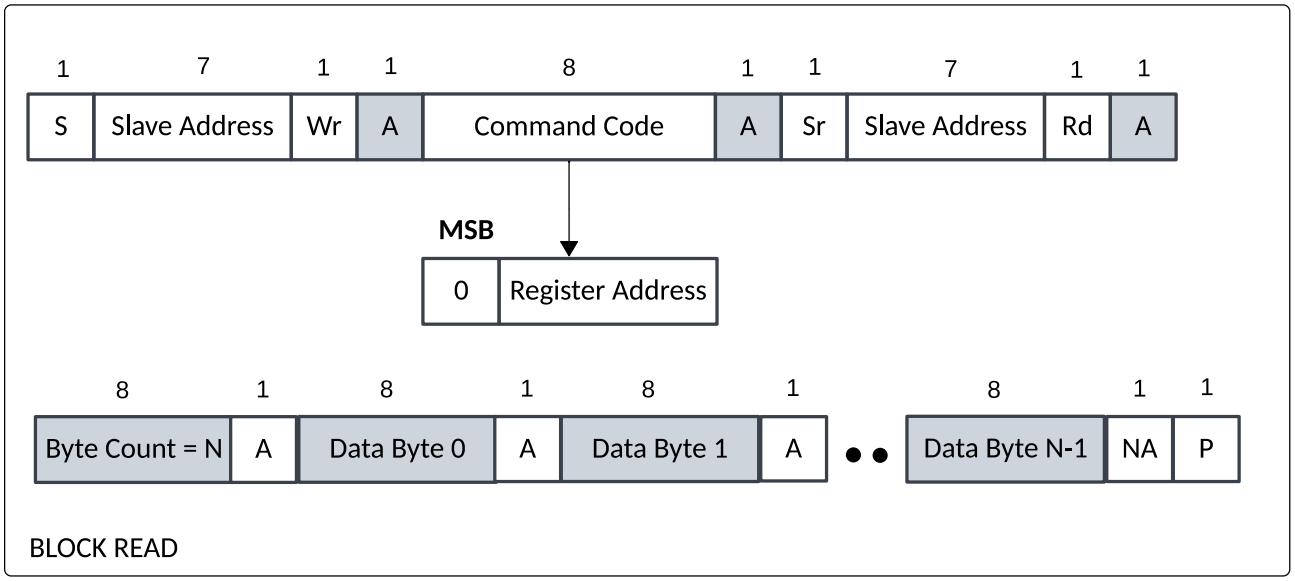



**Figure 13. Block Read Operation**

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 0 and block read starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends a repeated start bit
- Master sends the slave address with LSB = Read
- Slave device will send acknowledgement (A)
- Slave device will send byte count N (0 < N < 33) that slave will transfer to the master
- Master sends acknowledgement (A)
- Slave device sends data bytes from data byte 0 to data byte N-1
- Master will send acknowledgement (A) for each data byte received (one at a time) except for the last data byte (N-1)
- Master will send not-acknowledgment (NA)
- Master will send a stop bit

### Block Write

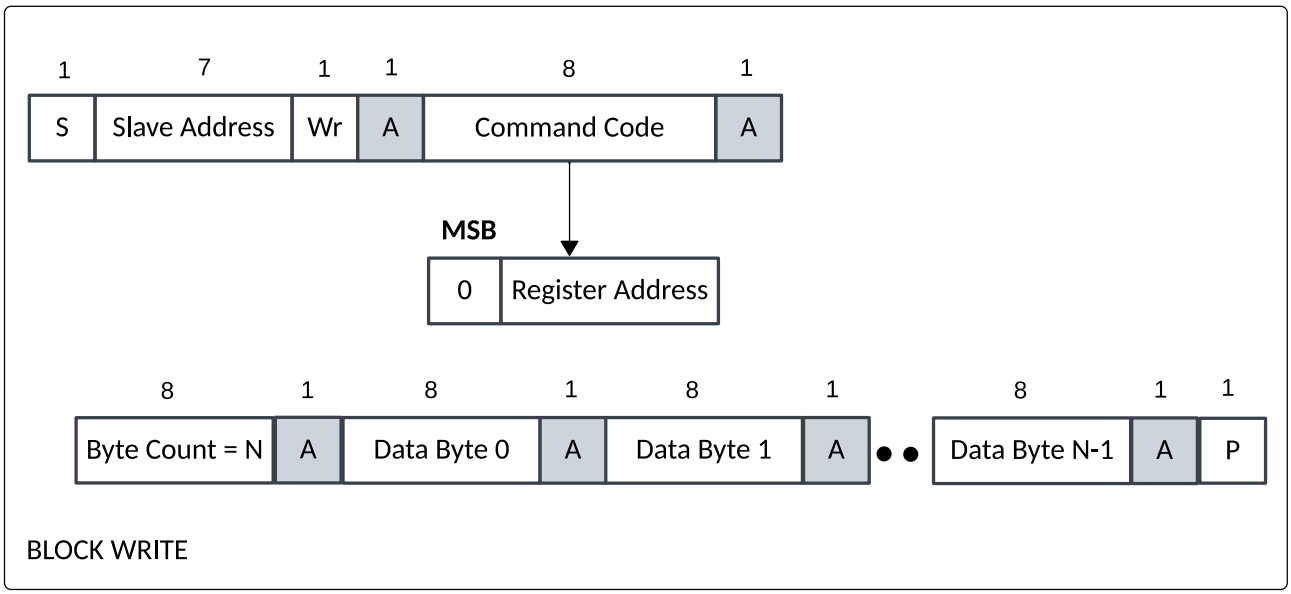



**Figure 14. Block Write Operation**

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 0 and block write starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends byte count N (0 < N < 33) that master will transfer to the slave device
- Slave device will send acknowledgement (A)
- Master sends data bytes to be written from data byte 0 to data byte N-1
- Slave device will send acknowledgement (A) for each data byte received (one at a time)
- Master sends a stop bit

**Note:** For cases where an SMBus bus transaction concludes with a write operation, ensure that the SMBus master does not toggle the clock inadvertently between the STOP and the next START condition to prevent unintended write operations. For cases where inadvertent clocks can occur between the STOP and the next START condition, it is recommended to conclude the SMBus transaction with a read operation.

### SMBus Address

The device has a default address of 0x6c (7-bit address).

## Register Address

### Table 13. Register Map Address

| Register Address | Bit Range | Register name | Default | Type | Bit Name | Description and Function |
|---|---|---|---|---|---|---|
| 0x00 | 7:0 | RCR1 | 0 | RO | RESERVED | |
| 0x01 | 7 | OE_CTRL 1 | 1 | RW | DIF5_ENABLE | 1: Output Enable<br>0: STOP_STATE Mode |
| | 6 | | 1 | | DIF4_ENABLE | |
| | 5 | | 1 | | DIF3_ENABLE | |
| | 4 | | 1 | | DIF2_ENABLE | |
| | 3 | | 0 | | RESERVED | |
| | 2 | | 1 | | DIF1_ENABLE | |
| | 1 | | 1 | | DIF0_ENABLE | |
| | 0 | | 0 | | RESERVED | |
| 0x02 | 7:3 | OE_CTRL 2 | 0 | RW | RESERVED | 1: Output Enable<br>0: STOP_STATE Mode |
| | 2 | | 1 | | DIF7_ENABLE | |
| | 1 | | 0 | | RESERVED | |
| | 0 | | 1 | | DIF6_ENABLE | |
| 0x03 | 7:0 | RCR2 | 0 | RO | RESERVED | |
| 0x04 | 7:0 | RCR3 | 0 | RO | RESERVED | |
| 0x05 | 7:4 | VEN_REV_ID | 0xa2 | RO | REVISION_ID | RevA : 0xa |
| | 3:0 | | | | VENDOR_ID | SiTime product : 0x2 |
| 0x06 | 7:0 | DEV_ID | 0 | RO | DEVICE_ID | Device ID bits[7:0] map to register bits[7:0] directly. Product Code |
| 0x07 | 7:5 | BYTES_READ_COUNT | 0 | RO | RESERVED | |
| | 4:0 | | 0x08 | RW | BYTES_READ_COUNT_VALUE | Writing to this register configures how many bytes will be read back on a block |
| 0x10 | 7 | OE_PIN_READ_BACK | 0 | RO | RB_OE7 | Output Enableb Pin read Back |
| | 6 | | 0 | | RB_OE6 | |
| | 5 | | 0 | | RB_OE5 | |
| | 4 | | 0 | | RB_OE4 | |
| | 3 | | 0 | | RB_OE3 | |
| | 2 | | 0 | | RB_OE2 | |
| | 1 | | 0 | | RB_OE1 | |
| | 0 | | 0 | | RB_OE0 | |
| 0x14 | 7:2 | STOP_STATE_CONFIG_REG | 0 | RO | RESERVED | |
| | 1:0 | | 0 | RW | STOP_STATE | 00 = Low/Low<br>01 = Hiz/Hiz<br>10 = High/Low<br>11 Low/High |
| 0x15 | 7:2 | SLEW_CTRL_REG | 0x01 | RO | RESERVED | |
| | 1:0 | | | RW | SLEW_RATE | Refer Table 14 |
| 0x16 | 7:4 | AMP_CTRL_REG | 0 | RO | RESERVED | |
| | 3:0 | | Refer note[1] | RW | OUTPUT_AMPLITUDE | Default Amplitude is 0.8 V peak typical.<br>Step size is 25 mV typical and monotically decreasing from code 0 to 15 |

**Note:**

1. For changing the default amplitude value, Readback the amplitude code and apply the relative change in code.

### Table 14. Default Slew Value

| Slew Code Reg. 0x15[1:0] | Typical Slewrate Value (V/ns) @ for 0.8V swing (measured on 10 inch T-line with 2pf load) |
|---|---|
| 0 | 3.8 |
| 1 | 2.9 |
| 2 | 2.4 |
| 3 | 2 |

## Package Dimensions and Land Pattern

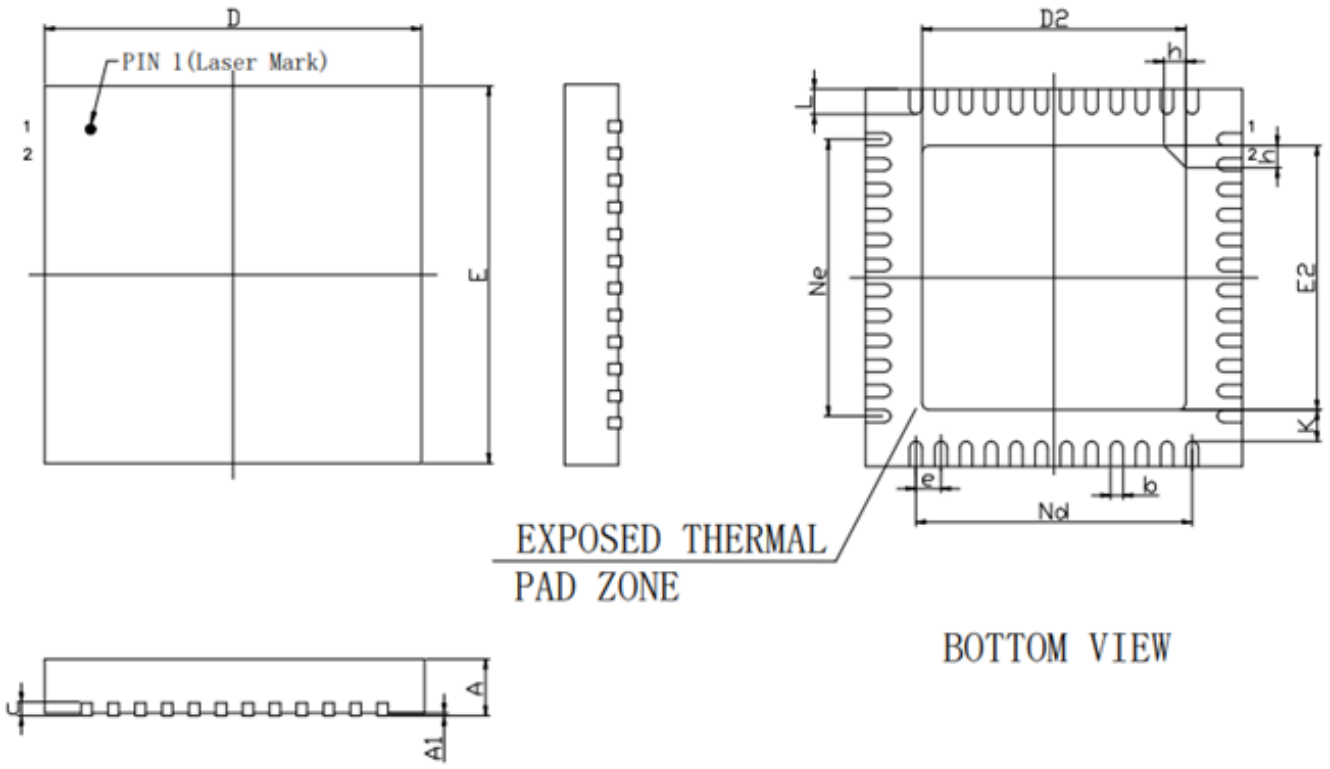



**Figure 15. Package Diagram SiT92318 48 pin VQFN**

| Symbol | Millimeter | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.95 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.23 |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 4.10 | 4.20 | 4.30 |
| e | 0.40 BSC | | |
| Ne | 4.40 BSC | | |
| Nd | 4.40 BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 4.10 | 4.20 | 4.30 |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | 0.50 | 0.55 |
| h | 0.30 | 0.35 | 0.40 |

**Notes:** All measurements are in millimeters (mm).

## Land Pattern and Solder

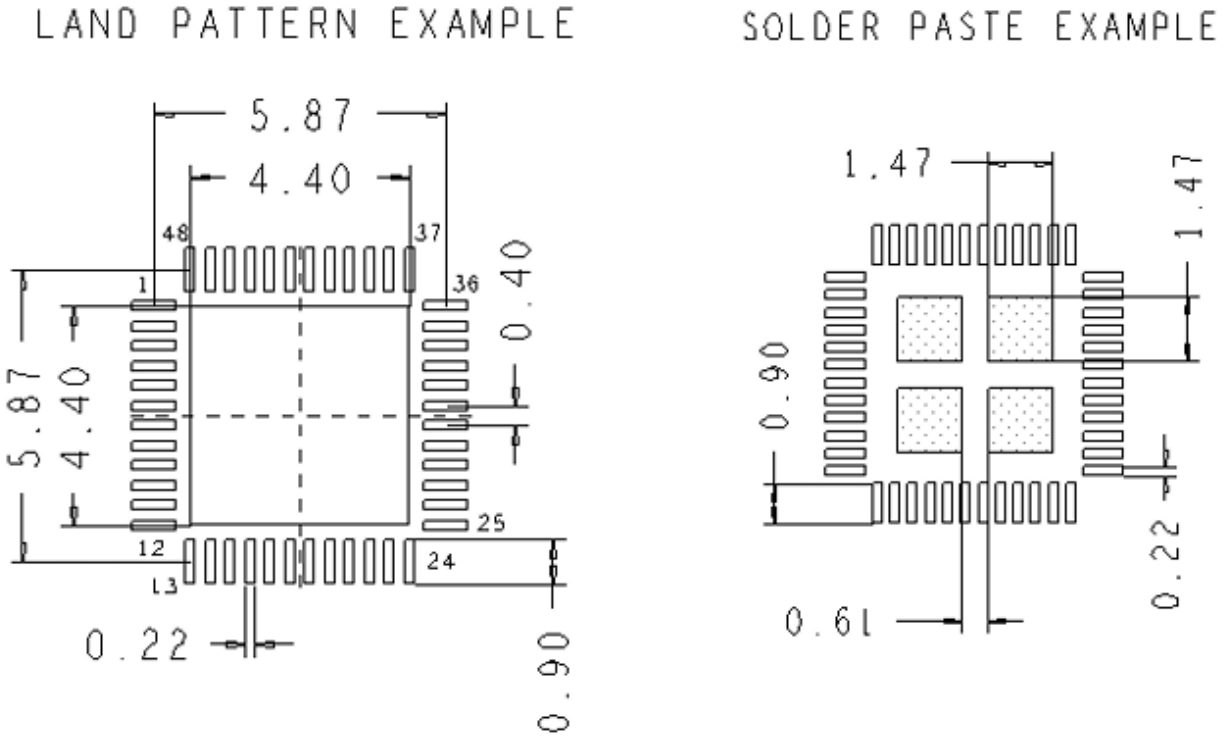



**Figure 16. SiT92318 Land Pattern Diagram**

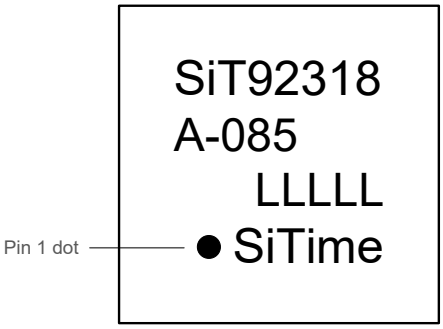
**General Notes**

2. All dimensions shown are in millimeters (mm) unless otherwise noted.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication allowance of 0.05 mm.

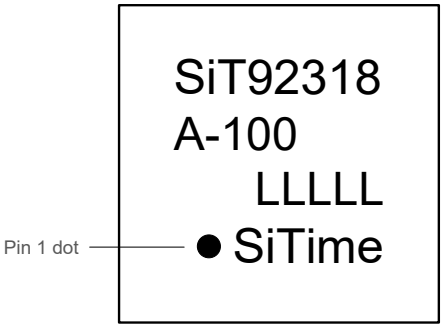
**SOLDER MASK DESIGN**

1. All metal pads are to be non-solder mask defined (NSMD).

## Top Marking




Line 1: “SiT92318” SiTime part number
Line 2: “A-085” represent revision A and 85 Ohm impedance
Line 3: “LLLLL” Lot code from SiTime
Line 4: Pin 1 dot and “SiTime” logo




Line 1: “SiT92318” SiTime part number
Line 2: “A-100” represent revision A and 100 Ohm impedance
Line 3: “LLLLL” Lot code from SiTime
Line 4: Pin 1 dot and “SiTime” logo

# Revision History

## Table 15. Revision History

| Revisions | Release Date | Change Summary |
|---|---|---|
| 0.5 | 11-Dec-2023 | Initial Release |
| 0.51 | 9-Jan-2025 | Updated with “P” reel code<br>Updated datasheet format |
| 0.54 | 21-Jan-2026 | Ordering Code for Packaging updated with 4Ku/reel code “P” and 500u/reel code “N”<br>Added Top Marking section;<br>Added 100 Ohm Termination option: 1st page Features; Headers; Ordering and Top Marking sections |
| 0.55 | 8-Apr-2026 | Datasheet tables have been updated to include support up to 105°C.<br>Land pattern is added<br>Additive jitter results with BRMC filter is added<br>Removed Top Marking Section<br>Updated disclaimer |
| 0.77 | 13-April-2026 | Revise additive phase jitter table format, remove top marking page |
| 0.9 | 28-July-2026 | Top marking updated , along with typical values of electrical specs |
| 1.0 | 3-Sep-2026 | Updated disclaimer<br>Top Marking updated<br>Production version |
| 1.01 | 10-Sep-2026 | Top marking udpated<br>Ordering Information updated |

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