SiT92216 4 Differential and 1 LVCMOS Output Ultra-Low Jitter High Performance Buffer

Description

The SiT92216 is a 4 differential outputs and 1 LVCMOS output ultra low-jitter clock fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution. The low impedance LVCMOS output is designed to drive 50 Ω series or parallel terminated transmission line.

The buffer can select a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock is distributed to 4 differential and 1 LVCMOS output drivers.

The SiT92216 operates from a 3.3 V / 2.5 V core supply and 3.3 V / 2.5 V output supply. HCSL and LVCMOS output driver can be operated at 1.8 V. The core supply and output supply are independent of each other and no supply sequencing is required.

Applications

- Carrier Ethernet
- 5G Wireless Base Stations, 5G Small Cells

Order samples

Features

- Additive jitter performance of 55 fs RMS
- 3:1 input clock selection
- Two universal clock inputs can operate up to 2.1 GHz and accept LVPECL, LVDS, LVCMOS, CML(ac-coupled only), HCSL, SSTL or single ended clocks
- One crystal input which can support crystals in the frequency range of 8 MHz to 50 MHz or it can accept single ended input clock.
- Two output driver banks A and B which can be programmed independently to LVPECL, LVDS, HCSL or HIZ mode.
- Output skew between clock outputs < 60 ps
- Level translation with core supply voltage of 3.3 V / 2.5 V and 3.3 V / 2.5 V output supply for differential output drivers
- 3.3 V/2.5 V/1.8 V operation for the single LVCMOS output driver and HCSL Driver
- SiT92216 buffer is pin controlled
- High PSRR -70/-73 dBc for LVPECL/LVDS modes
- Crystal input can be over driven with frequency up to 250 MHz in crystal bypass mode
- SiT92216 buffer is available in a 32-pin, 5 mm x 5 mm QFN package
- Support PCI-e Gen1 to Gen7

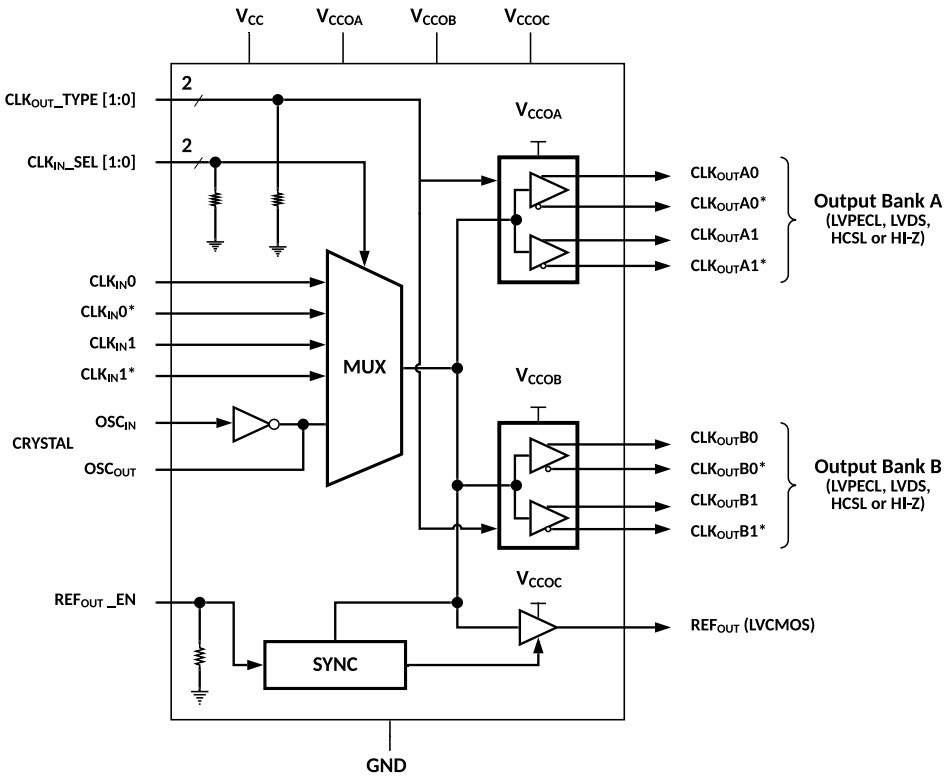

Figure 1. SiT92216 Block Diagram

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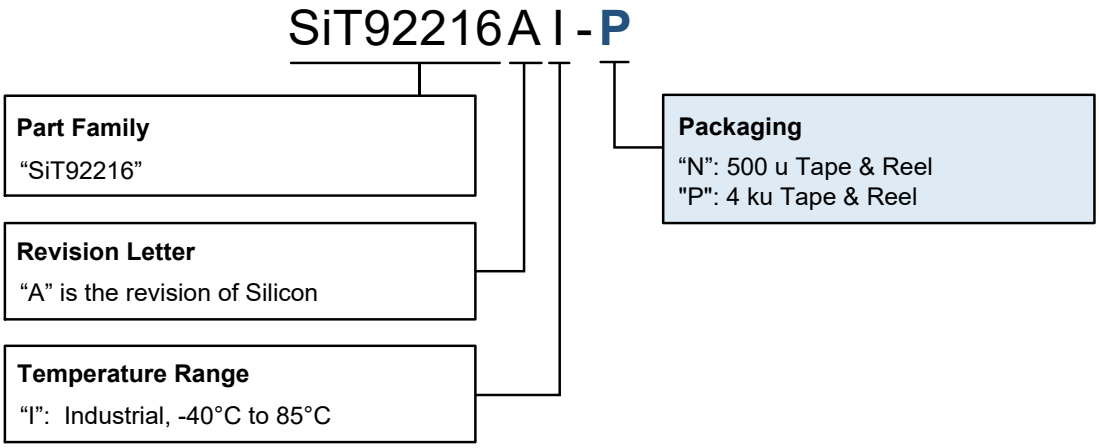
Ordering Information



Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Units
Core Supply Voltage, Analog Input	V_{CC}	-0.3		3.6	V
Output Bank Supply Voltage	V_{CCO}	-0.3		3.6	V
Input Voltage, All Inputs except OSC_{IN}	V_{IN}	-0.3		3.6	V
OSC_{IN}	V_{IN}	-0.3		1.5	V
Storage Temperature	TS	-55		150	°C
Moisture Sensitivity Level	MSL		3		

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Units
Core Supply Voltage	V_{CC}	3.135	3.3	3.45	V
	V_{CC}	2.375	2.5	2.625	V
Output Supply Voltage	$V_{CCOA/B}$	3.135	3.3	3.45	V
	$V_{CCOA/B}$	2.375	2.5	2.625	V
	$V_{CCOA/B}$[1]	1.71	1.8	1.89	V
Output Supply Voltage for LVCMOS Driver	V_{CCOC}	3.135	3.3	3.45	V
		2.375	2.5	2.625	V
		1.71	1.8	1.89	V
Ambient Temperature	T_A	-40		85	°C
Junction Temperature	T_J			125	°C

Note:

1. Only for HCSL.

Table 3. Electrical Characteristics

Unless otherwise specified: V_{CC} = 3.3 V ±5%, 2.5 V ±5%, V_{CCO}= 3.3 V ±5%, 2.5 V ±5%, -40 °C ≤ T_A ≤ 85°C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Core Supply Current, All Outputs Disabled	CLKIN0/1 selected	I_{CC_CORE}		16.5	19.8	mA
	XO selected	I_{CORE_XO}[3]		11.4	14	
Frequency Dependent Current Both Bank on Core Supply. This current scales with frequency	For F_{in} = 2100 MHz	I_{CC_DYN}[1,3]		25	33	mA
Increment in Core Supply when All ODR Banks are Enabled		$I_{CC\_ODR\_EN}$			2	mA
Additive Output Supply Current, LVPECL Banks Enabled		I_{CCO_PECL}		82	97.2	mA
Additive Output Supply Current, LVDS Banks Enabled		I_{CCO_LVDS}		40	49	mA
Additive Output Supply Current, HCSL Banks Enabled		I_{CCO_HCSL}		59	70.8	mA
Additive Output Supply Current, LVCMOS outputs Enabled	F_{IN} = 200 MHz, C_{LOAD} = 5 pF, V_{CCO} = 3.3 V	I_{CCO_CMOS}		6	7.2	mA
	F_{IN} = 200 MHz, C_{LOAD} = 5 pF, V_{CCO} = 2.5 V			4.5	5.5	

Notes:

1. Total current from core supply at frequency Fin = $I_{CORE,\ STATIC}$ + N*(0.5*$I_{CC\_ODR\_EN}$)+ N*(0.5*Fin/2100M)* $I_{CORE,\ DYN}$ Detailed methodology of calculating the power dissipated in each ODR mode is given in the section “Current consumption and Power Dissipation Calculations.” N is the number of output banks enabled.
2. Refer to Application Information Section for more information on current consumption and power dissipation calculations.
3. Specification is ensured by characterization and is not tested in production.

Table 4. Power Supply Ripple Rejection (PSRR)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Ripple-Induced Phase Spur Level Differential LVPECL Output	F_{IN} = 156.25 MHz, V_{CCO} = 2.5 V, 100 KHz offset, 100m Vpp	$PSRR_{LVPECL}$		-67		dBc
Ripple-Induced Phase Spur Level Differential LVDS Output		$PSRR_{LVDS}$		-70		
Ripple-Induced Phase Spur Level Differential HCSL Output		$PSRR_{HCSL}$		-67.7		

Notes:

1. Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [(2 * 10(PSRR / 20)) / (π * f_{CLK})] * $1E^{12}$
2. Specification is ensured by characterization and is not tested in production.

Table 5. Input Control Pin Characteristic

Parameter	Conditions	Symbols	Min	Typ	Max	Units
Input Low Current		I_{IL}	-20	0.1		µA
Input High Voltage – Logic Inputs		V_{IH}	0.7*V_{CC}		V_{CC}	V
Input Low Voltage – Logic Inputs		V_{IL}	GND		0.3*V_{CC}	V
Internal Pull-down Resistance		$R_{Pulldown}$		200		K Ω

Table 6. CMOS Control Inputs (CLK_{IN}_SELN, CLK_{OUT}_TYPEN, REF_{OUT}_EN)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Low Level Input Voltage		V_{IL}	GND		0.3*V_{CC}	V
High Level Input Voltage		V_{IH}	0.7*V_{CC}		V_{CC}	
High Level Input Current	V_{IH} = V_{CC} = 3.3 V	I_{IH}		30	50	uA
Low Level Input Current		I_{IL}	-20	0.1		

Table 7. CLOCK INPUTS (CLK_{IN}0/CLK_{IN}0*, CLK_{IN}1/CLK_{IN}1*)

Unless otherwise specified: Vcc = 3.3 V ± 5%, 2.5 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency Range[4]		F_{CLKin}	DC		2100	MHz
Differential Input High Voltage	CLK_{IN} driven differentially	V_{IHD}			V_{CC}	V
Differential Input Low Voltage		V_{ILD}	GND			V
Peak Differential Input Voltage Swing[2]		V_{ID}	0.15		1.3	V
Differential Input Common Mode Voltage	Input differential swing of 150 mV	V_{CMD}	0.25		V_{CC}-1.2	V
	Input differential swing of 350 mV		0.25		V_{CC}-1.1	V
	Input differential swing of 800 mV		0.25		V_{CC}-0.9	V
Single-Ended Input High Voltage	Inverting differential input held at V_{CC}/2, V_{CC} = 3.3 V	V_{IH}	2		V_{CC}	V
	Inverting differential input held at V_{CC}/2, V_{CC} = 2.5 V		1.6		V_{CC}	
Single-Ended Input Low Voltage	Inverting differential input held at V_{CC}/2, V_{CC} = 3.3 V	V_{IL}	GND		1.3	V
	Inverting differential input held at V_{CC}/2, V_{CC} = 2.5 V		GND		0.9	
Single-Ended Input Voltage Swing[3]		V_{I_SE}	0.3		Vcc	Vpp
Single-Ended Input Common Mode Voltage		V_{CM}	0.25		V_{CC}-1.2	V
Mux Isolation, CLK_{IN}0 to CLK_{IN}1	Fin = 100 MHz, Foffset > 50 KHz	ISO_{MUX}[1]		–84		dBc
	Fin = 200 MHz, Foffset > 50 KHz			–82		
	Fin = 500 MHz, Foffset > 50 KHz			–71		
	Fin = 1000 MHz, Foffset > 50 KHz			–65		

Table 8. Crystal Interface (OSC_{IN}, OSC_{OUT})

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Equivalent Series Resistance		ESR		35	60	Ω
Load Capacitance		CL	6	8	10	pF
Shunt Capacitance		Co		2	3	pF
Power Dissipated in the Crystal		Drive level		100	200	uW
Mode of Oscillation				Fundamental		
Crystal Frequency Range		F_{OSC}[1]	8		50	MHz
External Clock Frequency Range	XO over drive or Bypass mode	F_{CLK}			250	MHz
Maximum Swing Level on OSC_{IN}/OSC_{OUT} Pins	XO over drive or Bypass mode	Vmax			1.8	V
Crystal Phase Jitter [4]	RMS, integration BW 12 kHz to 5 MHz, $F_{crystal}$ = 25 MHz. Crystal input select Measured at V_{CC} = V_{CCO} = 2.5 V	t_{jit}[1]		155		fs(rms)
External Clock Frequency Range	XO over drive or Bypass mode	F_{CLK}			250	MHz

Notes:

1. Specification is ensured by characterization and is not tested in production.
2. Refer to Parameter Measurement Information for definition of VID and VOD voltages.
3. If the input clock is initially absent when the chip is just powered up, it will take atleast 2 falling edges of clock cycle for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edges of input clock.
4. Crystal Phase Jitter is measure on following part number, 7M-25.000MAKV-T.

Table 9. LVPECL OUTPUTS ($CLK_{OUT}An/CLK_{OUT}An^*$, $CLK_{OUT}Bn/CLK_{OUT}Bn^*$)

Unless otherwise specified: Vcc = 3.3 V ± 5%, 2.5 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, $CLK_{IN}0/1$ driven differentially, input slew rate ≥3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C. Termination is 50 Ω to V_{CCO} -2V.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Maximum Output Frequency Full VOD Swing	Maximum output frequency, full VOD swing ≥ 600 mV 50 Ω termination biased with V_{CCO} -2V	F_{CLKOUT_FS}	1000	1200		MHz
Maximum Output Frequency Reduced VOD Swing	Maximum output frequency, full VOD swing ≥ 400 mV 50 Ω termination biased with V_{CCO} -2V		1500	2100		MHz
Additive RMS Jitter Freq = 156.25M ; Integration Bandwidth 12 kHz to 20 MHz	Integration bandwidth from 12 KHz to 20 MHz, FIN = 156.25 MHz, SR > 3 V/ns 50 Ω termination biased with V_{CCO}-2V, FIN = 156.25 MHz, SR > 3 V/ns	$Jitter_{ADD}$		55	88	fs(rms)
Noise Floor f_{OFFSET} ≥ 10 MHz	50 Ω termination biased with V_{CCO}-2V, FIN = 156.25 MHz, SR > 3 V/ns	$Noise_{FLOOR}$		-159		dBc/Hz
Duty Cycle	50 Ω termination biased with V_{CCO} -2V	ODC	45		55	%
Output High Voltage	50 Ω termination biased with V_{CCO} -2V	V_{OH}	V_{CCO} – 1.165		V_{CCO} – 0.75	V
Output Low Voltage	50 Ω termination biased with V_{CCO} -2V	V_{OL}	V_{CCO} – 2.0		V_{CCO} – 1.45	V
Output Voltage Swing	50 Ω termination biased with V_{CCO} -2V	V_{OD}	0.5		0.86	V
Output Rise Time 20% to 80%	50 Ω termination biased with V_{CCO} -2V	t_R		210	350	ps
Output Fall Time 80% to 20%	50 Ω termination biased with V_{CCO} -2V	t_F		210	350	ps

Table 10. LVDS Outputs ($CLK_{OUT}An/CLK_{OUT}An^*$, $CLK_{OUT}Bn/CLK_{OUT}Bn^*$)

Unless otherwise specified: V_{CC} = 3.3 V ±5%, 2.5 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%, -40°C ≤ T_A ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Maximum Output Frequency, full VOD swing ≥ 250 mV	R_L = 100 Ω, differential	F_{CLKOUT_FS}[1]	1000	1600	-	MHz
Maximum Output Frequency, full VOD swing ≥ 200 mV	R_L = 100 Ω, differential		1500	2100		MHz
Additive RMS Jitter[1]	Integration bandwidth from 12 KHz to 20 MHz, Fin = 156.25 MHz, SR > 3 V/ns RL = 100 Ω, differential	$Jitter_{ADD}$		60	82	fs(rms)
Noise Floor f_{OFFSET} ≥ 10 MHz	Fin = 156.25 MHz, SR > 3 V/ns RL = 100 Ω, differential	$Noise_{FLOOR}$		-159		dBc
Duty Cycle	RL = 100 Ω, differential	ODC	45		55	%
Output Differential Peak Voltage	R_L = 100 Ω, differential, 156.25M	V_{OD}	300		420	mV
Change in Magnitude of VOD for Complementary Output States	RL = 100 Ω, differential	ΔV_{PP}			50	mV
Output Offset Voltage	LVDS common mode	V_{OS}	1.125	1.25	1.375	V
Change in Magnitude of VOS for Complementary Output States		ΔV_{OS}			50	mV
Output Short Circuit Current Single Ended					9.6	mA
Output Short Circuit Current Differential					9.6	mA
Output Rise Time 20% to 80%	RL = 100 Ω, differential, CL < 5 pF	t_R		210	350	ps
Output Fall Time 80% to 20%	Uniform transmission line up to 10 inches with characteristic impedance of 50 Ω	t_F		210	350	ps
Input to Output Delay		t_{pd}		840	1100	ps
Skew between Outputs from same Bank (Absolute max)Skew between Outputs	V_{CCO} = 3.3 V, 2.5 V_{CCO} = 3.3 V, 2.5 V	T_{sk}		30	60	ps

Notes:

1. Specification is guaranteed by characterization and is not tested in production.

Table 11. LVCMOS Output (REF_{OUT})

Unless otherwise specified: V_{CC} = 3.3 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%,1.8 V ±5%, -40 °C ≤ T_A ≤ 85°C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Frequency		f_{CLKOUT}	0		250	MHz
Additive RMS Jitter Freq = 156.25M; Integration Bandwidth 12 kHz to 20 MHz	V_{CCOC} = 3.3 V ±5%	$Jitter_{ADD}$[1]		30	50	fs rms
	V_{CCOC} = 2.5 V ±5%			40	60	
	V_{CCOC} = 1.8 V ±5%			90	150	
Output Duty Cycle	For Fin ≤ 200 MHz	ODC	45		55	%
	For 200 MHz < Fin < 250 MHz		40		60	%
Output High Voltage	V_{CCOC} = 3.3 V ±5%, 1 mA pull down current	V_{OH}	V_{CCOC} -0.1 V			V
	V_{CCOC} = 2.5 V ±5%, 1 mA pull down current		V_{CCOC} -0.1 V			V
Output Low Voltage	V_{CCOC} = 3.3 V ±5%, 1 mA pull up current	V_{OL}			0.1	V
	V_{CCOC} = 2.5 V ±5%, 1 mA pull up current				0.1	V
Output Rise Time, 20% to 80%	C_{LOAD} = 5 pF, R_{LOAD} = 50 Ω AC coupled	t_R		250	450	ps
Output Fall Time 20% to 80%		t_F		250	450	ps
Output Enable Time		t_{EN}[1]			4	cycles
Output Disable Time		t_{DIS}[1]			4	cycles
Input to Clock Edge to Output Clock Edge Delay	V_{CCO} = 3.3 V, PCB trace of 5 inch, 5 pF capacitor	t_d[1]		1.4	2.5	ns
	V_{CCO} = 2.5 V, PCB trace of 5 inch, 5 pF capacitor			1.5	2.7	ns

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 12. HCSL Outputs ($CLK_{OUT}An/CLK_{OUT}An^*$, $CLK_{OUT}Bn/CLK_{OUT}Bn^*$)

Unless otherwise specified: V_{CC} = 3.3 V ±5%, 2.5 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%,1.8 V ±5% -40°C ≤ T_A ≤ 85°C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Frequency Range	R_L= 50 Ω to GND	F_{CLKOUT_FS}	DC		700	MHz
Additive RMS Jitter[1]	Integration bandwidth from 12 kHz to 20 MHz, F_{IN} = 156.25 MHz, SR > 3 V/ns R_L = 50 Ω to GND	$Jitter_{ADD}$		55	86	fs(rms)
Noise Floor f_{OFFSET} ≥ 10 MHz		$Noise_{FLOOR}$		-159		dBc
Output Duty Cycle		ODC	45		55	%
Output Low Voltage Min	R_L = 50 Ω to GND at far end; 50 Ω controlled impedance transmission line Supply voltage: 1.8 V ±5%), 2.5 V (±10%), 3.3 V (±10%)	V_{MIN} (transient)	-200			mV
Single-ended Output High Voltage	R_L = 50 Ω to GND	V_{OH}	600	840	1150	mV
Single-ended Output Low Voltage		V_{OL}	-150	28	150	mV
Absolute Crossing Voltage	R_L = 50 Ω to GND, C_L < 5 pF	V_{CROSS}	250		550	mV
Total Variation of V_{CROSS}		$V_{CROSSDELTA}$			140	mV

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Skew between P and N rails	R_L = 50 Ω to GND at far end; 50 Ω controlled impedance transmission line; PCB routing skew <1 ps Supply voltage: 2.5 V (±10%), 3.3 V (±10%)	$P\text{-}N_{SKEW}$	< abs (50)			ps
Output Rise Time 20% to 80%	F_{IN} = 156.25 MHz, Uniform transmission line up to 10 inches with characteristic impedance of 50 Ω R_L = 50 Ω to GND, C_L < 5 pF	t_R		210		ps
Output Fall Time 80% to 20%		t_F		210		ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 13. Propagation Delay and Output Skew

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Propagation Delay CLK_{IN}-to-LVPECL	50 Ω termination biased with V_{CCO} -2 V	t_{PD}	723	818	931	ps
Propagation Delay CLK_{IN}-to-LVDS		t_{PD}	726	826	944	ps
Propagation Delay CLK_{IN}-to-HCSL		t_{PD}	705	820	897	ps
Propagation Delay CLK_{IN}-to-LVCMOS	V_{CCO} = 3.3 V, PCB trace of 5 inch, 5 pF capacitor	t_D[1]		1.4	2.5	ns
	V_{CCO} = 2.5 V, PCB trace of 5 inch, 5 pF capacitor			1.5	2.7	ns
Output Skew LVPECL/LVDS/HCSL	V_{CCO} = 3.3 V, 2.5 V	Tsk(o)[1]			60	ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 12. ESD Ratings

Parameter	Conditions	Symbol	Value	Units
Electrostatic Discharge	Human Body Model		±2000	V
	Charged Device Model		±1500	

Table 13. Thermal Characteristics

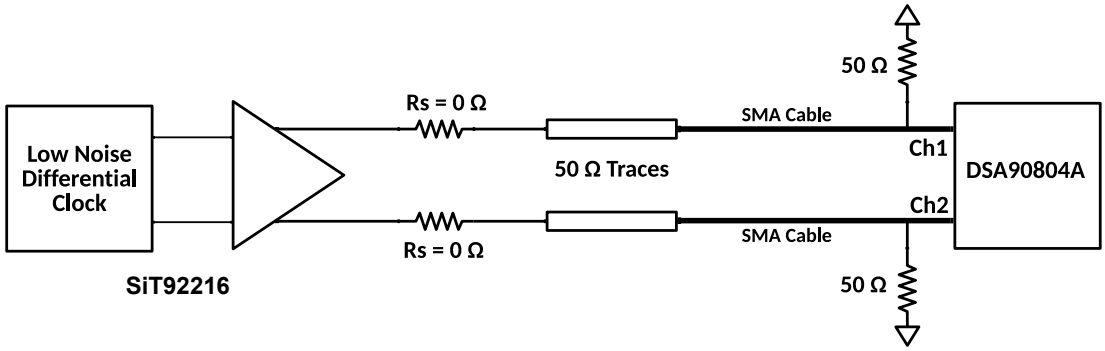
Parameter	Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Resistance	θ_{JA}		37.4		°C/W
Junction to Board	θ_{JB}		16.62		°C/W
Junction to Case	θ_{JC}		23.7		°C/W
Junction to Top Characterization Parameter	ψ_{JT}		0.75		°C/W

Table 14. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architecture

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	PCIe Gen 1[1,2,3,4]	$t_{jphPCIeG1-CC}$		2	5	ps (p-p)
	PCIe Gen 2[1,2,3,4]	$t_{jphPCIeG2-CC}$		0.08	0.15	ps(rms)
	PCIe Gen 3[1,2,4,6]	$t_{jphPCIeG3-CC}$		0.03	0.07	
	PCIe Gen4[1,2,4,6]	$t_{jphPCIeG4-CC}$		0.03	0.07	
	PCIe Gen5[1,2,4,6]	$t_{jphPCIeG5-CC}$		0.01	0.022	
	PCIe Gen6[1,2,4,6]	$t_{jphPCIeG6-CC}$		0.008	0.014	
	PCIe Gen7[1,2,4,6]	$t_{jphPCIeG7-CC}$		0.006	0.01	

Notes:

1. Applies to all the differential outputs, gauranteed by design and characterization.
2. Applies to all the Outputs when driven by a low phase noise source SMA100B.
3. Additive RMS Jitter Measurements were made using DSA90804A for minimum waveform length of ≥ 100k cycles with a minimum sampling rate of ≥ 40GSa/s with the waveform covering 90% of the DSO screen. All the post processing the DSO is disabled to decrease the additonal jitter impact from oscilloscope. Broadband oscilloscope noise is also minimized in the measurement.
4. Additive jitter for RMS values is calculated by solving the equation for b [b=sqrt(c^2-a^2)] where ‘a’ the rms input jitter and “c” is the rms total jitter.
5. Input to SiT92216 is fed using low phase noise source SMA100B, SiT92216 is configured as 100 MHz HCSL Output Driver [VCCOx = 3.3 V] and fed to the channels of DSA90804A using the exact measurement set up [Refer Note 6].
6. SiT92216 PCI Express Additive RMS Jitter Measurement Set up configuration.



Pin Description

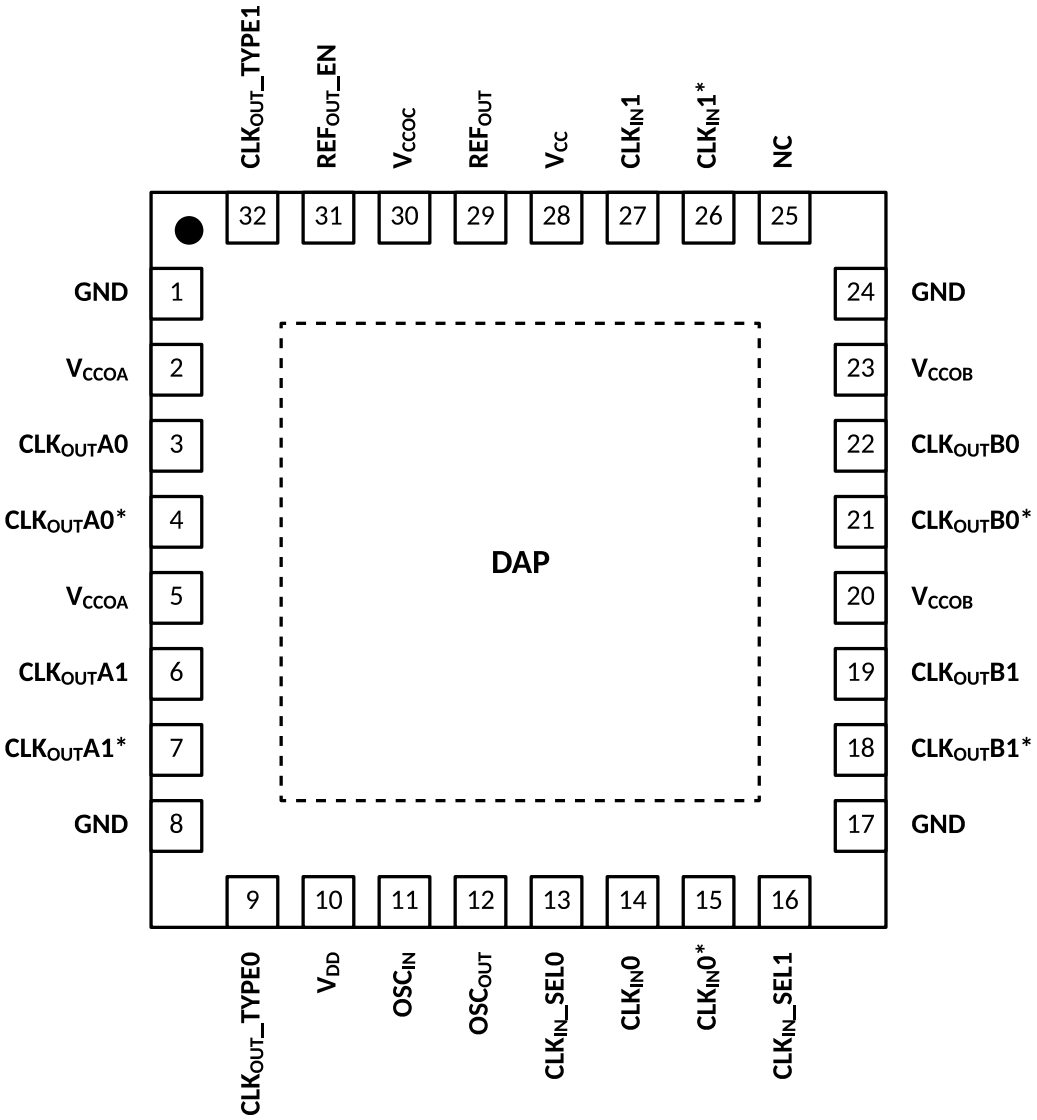


Figure 2. SiT92216 Top View

Table 15. Detailed Pin Description

Pin Name	I/O Type	Pin No	Function
DAP	GND	DAP	Die Attach Pad. Connect to the PCB ground plane for heat dissipation
GND	GND	1,8,17, 24	Ground
V_{CCOA}	Power	2, 5	Power supply for Bank A Output buffers. V_{CCOA} operates from 3.3 V or 2.5 V. 1.8 V is supported for HCSL driver. The V_{CCOA} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each V_{CCO} pin. [2]
$CLK_{OUT}A0$,	Output	3	Differential clock output A0. Output type set by CLK_{OUT}_TYPE pins
$CLK_{OUT}A0$*		4	
$CLK_{OUT}A1$	Output	6	Differential clock output A1. Output type set by CLK_{OUT}_TYPE pins.
$CLK_{OUT}A1$*		7	
CLK_{OUT}_TYPE0	Power	9	Bank A and Bank B output buffer type selection pins[3]
CLK_{OUT}_TYPE1		32	

Pin Name	I/O Type	Pin No	Function
V_{CC}	Input	10, 28	Power supply for Core and Input Buffer blocks. The V_{CC} supply operates from 3.3 V or 2.5 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each V_{CC} pin.
OSC_{IN}	Input	11	Input for crystal can also be driven by a XO, TCXO, or other external single-ended clock
OSC_{OUT}	Output	12	Output for crystal. Leave OSC_{OUT} floating if OSC_{IN} is driven by a single ended clock.
CLK_{IN}_SEL0	Input	13	Clock input selection pins[3]
CLK_{IN}_SEL1		16	
CLK_{IN}0	Input	14	Universal clock input 0 (differential/single-ended)
CLK_{IN}0*		15	
CLK_{OUT}B1*	Output	18	Differential clock output B1. Output type set by CLK_{OUT}_TYPE pins
CLK_{OUT}B1		19	
V_{CCOB}	Power	20, 23	Power supply for Bank B Output buffers. VCCOB operates from 3.3 V or 2.5 V. 1.8 V is supported for HCSL driver. The VCCOB pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each V_{CCO} pin.
CLK_{OUT}B0*	Output	21	Differential clock output B0. Output type set by CLK_{OUT}_TYPE pins
CLK_{OUT}B0		22	
NC		25	Not Connected
CLK_{IN}1*	Input	26	Universal clock input 1 (differential/single-ended)
CLK_{IN}1		27	
REF_{OUT}	Output	29	LVCMOS reference output. Enable output by pulling REF_{OUT}EN pin high.
V_{CCOC}	Power	30	Power supply for REF_{OUT} buffer. V_{CCOC} operates from 3.3 V or 2.5 V or 1.8 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each V_{CCO} pin.[2]
REF_{OUT}_EN	Input	31	REF_{OUT} enable input. Enable signal is internally synchronized to the selected clock input[3]

Functional Description

Functional Block Diagram

The SiT92216 is a 4 differential outputs, 1 LVCMOS clock output fan out buffer with ultra-low additive jitter that can operate up to 2.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 4 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 32-pin WQFN package.

The SiT92216 has separate 3.3 V/2.5 V core (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}). HCSL can support 1.8 V output power supplies (V_{CCOA}, V_{CCOB}). V_{CCOC} supply can operate on 3.3 V/2.5 V/1.8 V rail. Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to its respective V_{CCO} supply, while the output levels for LVDS and HCSL are relatively constant over the specified V_{CCO} range.

Vcc and Vcco Power Supplies

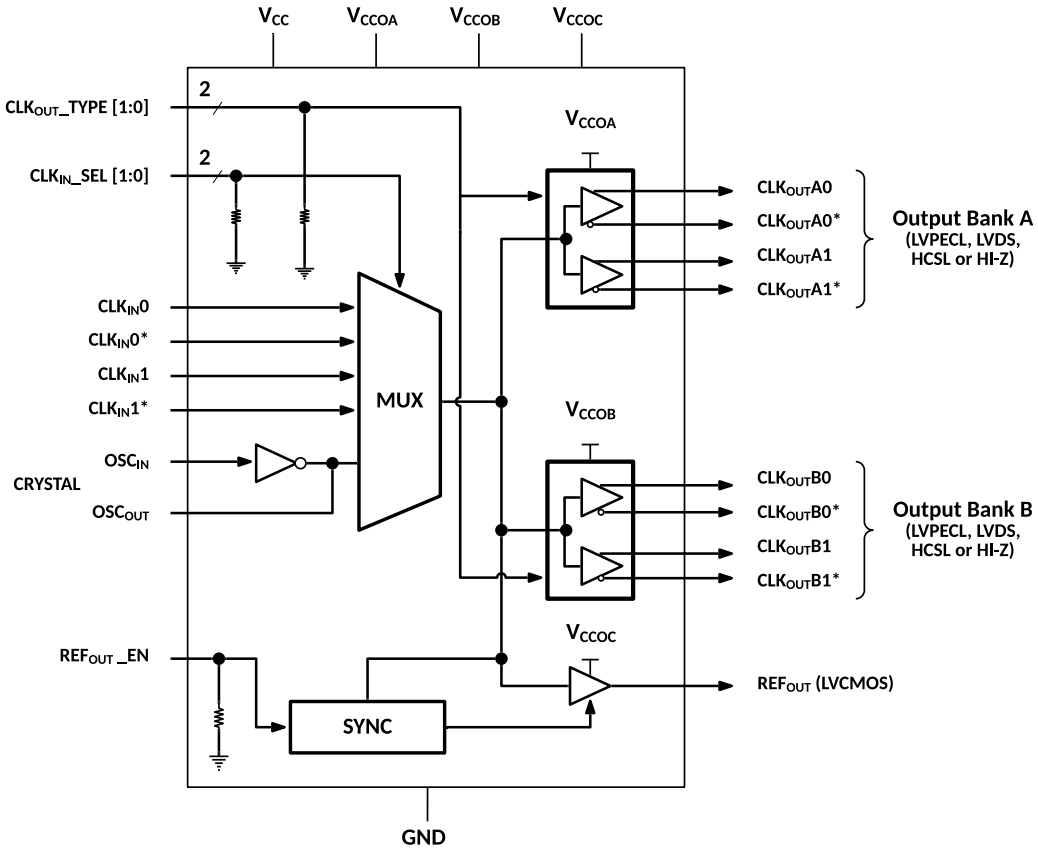


Figure 3. Functional Block Diagram

Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, $CLK_{IN}1$/$CLK_{IN}1$*, or OSC_{IN}. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in Table 16. When $CLK_{IN}0$ or $CLK_{IN}1$ is selected, the oscillator is powered down. The user can float OSCin and OSCout pins, since these pins are internally pulled down. OSCin is pulled down with a 56 KΩ resistance.

Table 16. Input Clock Selection

CLKin_SEL[1]	CLKin_SEL[0]	Selected Clock
0	0	$CLK_{IN}0$, $CLK_{IN}0$*
0	1	$CLK_{IN}1$, $CLK_{IN}1$*
1	0	Crystal or Crystal bypass AC coupled mode
1	1	Crystal bypass DC coupled mode

Clock States (Input vs Output States)

Table 17. Input versus Output Stages

State of Selected Clock input	Output State
Inputs are floating	Logic low
Inputs are logic low	Logic low
Inputs are logic high	Logic high

Output Driver Type

The differential output buffer type for Bank A and Bank B outputs can be configured using the CLK_{OUT}_TYPE[1:0] inputs, respectively, as shown Table 18. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, it is recommended to disable (Hi-Z) the bank to reduce power.

Table 18. Programming of Output Driver Type

CLK_{OUT}_TYPE1	CLK_{OUT}_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HI-Z

Reference Output

The reference output (REF_{OUT}) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the V_{CCOC} voltage. REF_{OUT} can be enabled or disabled using the enable input pin, REF_{OUT}_EN, as shown in Table 19. The reference output clock is internally synchronized to the selected clock. This avoids any glitches or runt pulses while enabling or disabling the reference clock. Pulling REF_{OUT}_EN to LOW forces the outputs to the high-impedance state within 4 falling edges of the input signal. The outputs remain in the high-impedance state as long as REF_{OUT}_EN is LOW. When REF_{OUT}_EN goes from HIGH to LOW, the output clock is disabled within 4 falling edges of the input clock signal. The output is disabled at the falling edge of the input clock. This allows the output clock to be disabled in a glitch-free manner.

When REF_{OUT}_EN goes from low to high, the output clock is enabled within a time delay td, where td is given by the following equation.

$$t_{d,refout\_en} = 0.5n + 3 * T_{in}.$$

T_{in} is the time period of the input clock.

When REF_{OUT}_EN is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REF_{OUT}_EN is configured with a 1K Ω load to ground, then the output will be pulled to low when disabled.

Table 19. Reference Output Enable

REF_{OUT}_EN	Output State
0	Disabled (Hi-Z)
1	Enabled

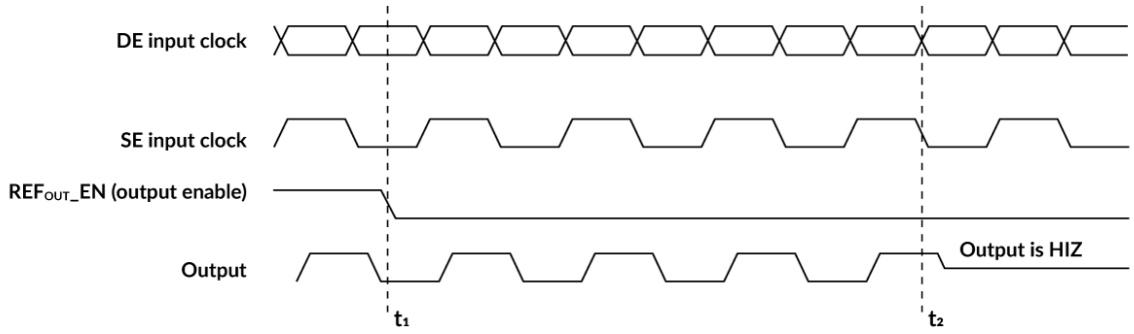


Figure 4. REF_{OUT}_EN: output disable

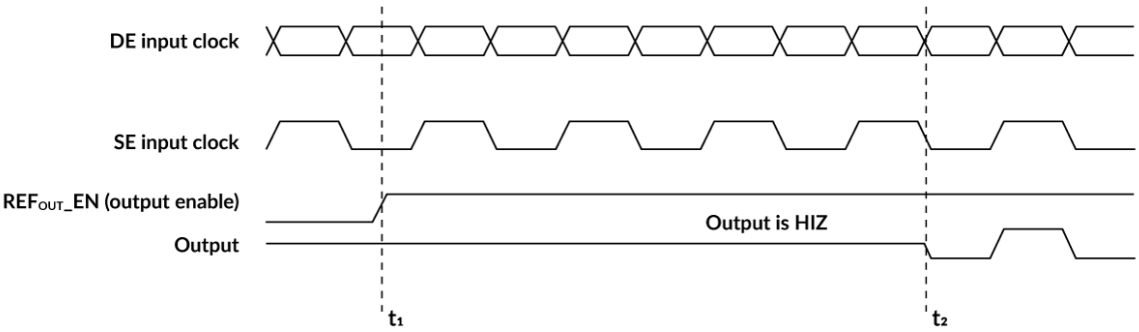


Figure 5. REF_{OUT}_EN: output enable

Application Information

Current Consumption and Power Dissipation Calculations

The current consumption specified in the Electrical Characteristics can be used to calculate the total power dissipation and the IC power dissipation for any output driver configuration. The total current drawn from the V_{CC} is given by the equation below.

$$I_{CC} = I_{CORE,STATIC} + N * (0.5 * I_{ODR_{ENABLE}}) + N * \left(0.5 * \frac{f_{in}}{2.1G}\right) * I_{CORE,DYN}$$

- I_{CC} is the total core current drawn from V_{CC}.
- $I_{CORE,STATIC}$ is the current taken from V_{CC}, when no clocks are toggling and both the output driver banks are in HI-Z state.
- I_{ODR_ENABLE} is the increment current taken from V_{CC} if all ODR banks are enabled.
- $I_{CORE,DYN}$ is the switching current taken from V_{CC} when the selected input clock is toggling at a frequency of f_{in}(Hz).
- N is the number of output banks enabled.

Currents consumed by the output supplies in each mode are listed below. The current for output bank A/B in LVPECL mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC\_LVPECL}$$

The current for output bank A/B in LVDS mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC\_LVDS}$$

The current for output bank A/B in HCSL mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC\_HCSL}$$

The current for output bank C is given below.

$$I_{CCOC} = I_{CC\_LVCMOS}$$

The equation for the total power dissipation is given below.

$$P_{TOTAL} = V_{CC} * I_{VCC} + V_{CCOA} * I_{CCOA} + V_{CCOB} * I_{CCOB} + V_{CCOC} * I_{CCOC}$$

If the output driver configuration is LVPECL or LVDS, then the power dissipated in any termination resistors and termination voltages needs to be accounted to calculate the power dissipation in the device.

The power dissipated in the termination resistors in LVPECL mode is given below.

$$P_{RT\_PECL} = \frac{(V_{OH\_PECL} - V_{TT})^2}{R_T} + \frac{(V_{OL\_PECL} - V_{TT})^2}{R_T}$$

The power dissipated in the termination voltage for LVPECL mode is given below

$$P_{VTT\_PECL} = V_{TT} * \left(\frac{(V_{OH\_PECL} - V_{TT})}{R_T} + \frac{(V_{OL\_PECL} - V_{TT})}{R_T}\right)$$

The power dissipated in the ground referenced termination resistor for HCSL is given below.

$$P_{RT\_HCSL} = \frac{V_{OH\_HCSL}^2}{R_T}$$

The power dissipated in the device is given below.

$$P_{DEVICE} = P_{TOTAL} - N_1 * (P_{RT_{PECL}} + P_{VTT_{PECL}}) - N_2 * P_{RT\_HCSL}$$

where

- N1 is the number of LVPECL output pairs with termination resistors to V_{TT} (usually Vcco-2V).
- N2 is number of HCSL output pairs with termination resistors to GND.

Example: Worst case power dissipation
Output drivers of Banks A and B are configured in LVPECL mode. The input frequency is 2100 MHz. V_{CC} = 3.465 V, V_{CCOA} = V_{CCOB} = V_{CCOC} = 3.465 V, REF_{OUT} is enabled. Assume 5 pF load for REF_{OUT}.

Table 20. Worst case power dissipation

Parameter	Value	Unit
V_{CC}	3.465	V
V_{CCOA}	3.465	V
V_{CCOB}	3.465	V
V_{CCOC}	3.465	V
I_{CC}	49	mA
I_{CCOA}	84	mA
I_{CCOB}	84	mA
I_{CCOC}	10	mA
P_{TOTAL}	569	mW
V_{OH_PECL}	2.5	V
V_{OL_PECL}	1.8	V
V_{TT}	1.465	V
P_{RT_PECL}	23.6	mW
P_{VTT_PECL}	40	mW
P_{DEVICE}	532	mW

Driving the Clock Inputs

The SiT92216 has two universal clock inputs ($CLK_{IN}0/CLK_{IN}0^*$ and $CLK_{IN}1/CLK_{IN}1^*$). SiT92216 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The SiT92216 supports a wide common mode voltage range and input signal swing.

To achieve optimal phase noise and jitter performance, the input must have a high differential slew rate of 3 V/ns or greater. Driving the input with a lower slew rate will degrade the noise floor and jitter.

It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say $CLK_{IN}0$, then $CLK_{IN}0^*$ pin needs to be connected to a 0.1 uF capacitor on the PCB.

Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 6 illustrates how a differential input can be configured to accept LVCMOS single-ended signals using AC coupling. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass capacitor should be located as close to the input pin as possible. Two resistors R_{T1} and R_{T2} set the common mode voltage at the output of the LVCMOS driver to $V_{CC}/2$. This prevents DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{T1} and R_{T2} values should be adjusted to set the V1 at 1.25 V. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

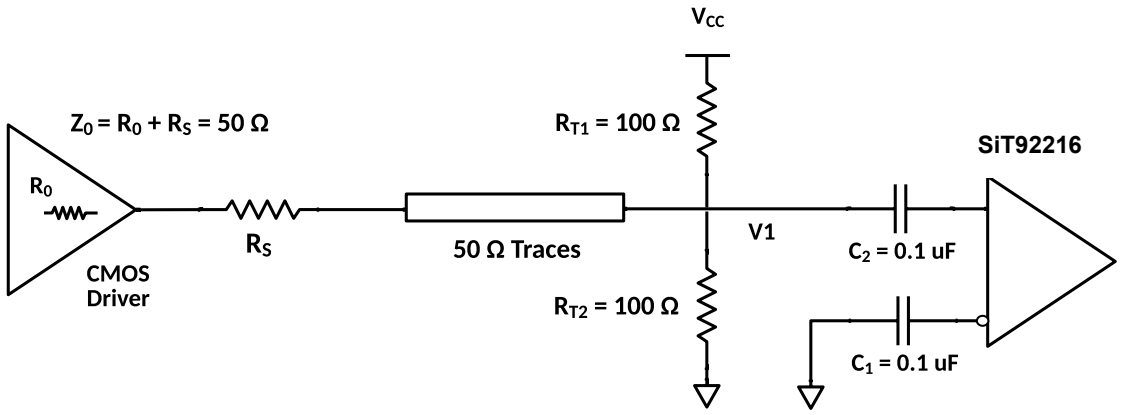


Figure 6. AC coupling LVCMOS clock to SiT92216

The inverting differential input can be connected to a 0.1 uF bypass capacitor. This pin is biased internally to a voltage close to $V_{CC}/2$.

Another variant of the AC coupling of LVCMOS input clock is shown in Figure 7. We use single termination resistor of 50 Ω to ground. A 0.1 uF (C_3) AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50\ \Omega$$

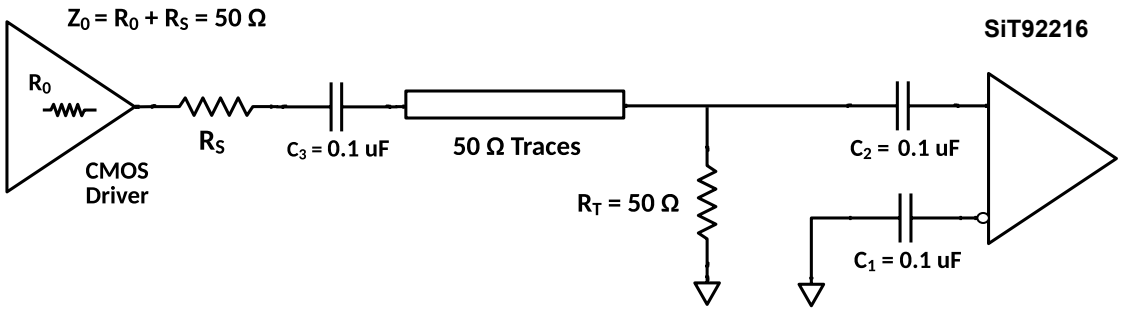


Figure 7. AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

Driving Clock Inputs with LVCMOS Driver (DC coupled)

Figure 8 illustrates how a differential input can be configured to accept LVCMOS single-ended signals using DC coupling. The reference voltage V1 = $V_{CC}/2$ is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vcc}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

$$Z_o = R_o + R_s = 50\ \Omega$$

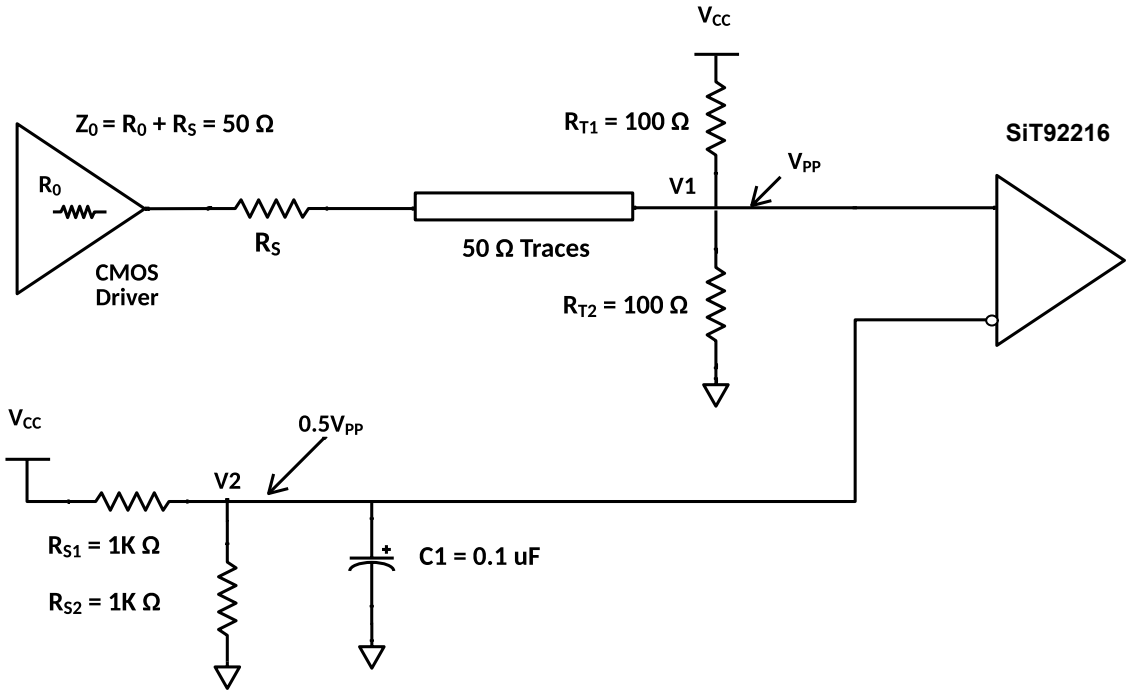


Figure 8. DC coupling of LVCMOS clock to SiT92216 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values below are for when both the single ended swing and V_{CC} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 9 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor RT to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50 Ω load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 9 is given below

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2}$$

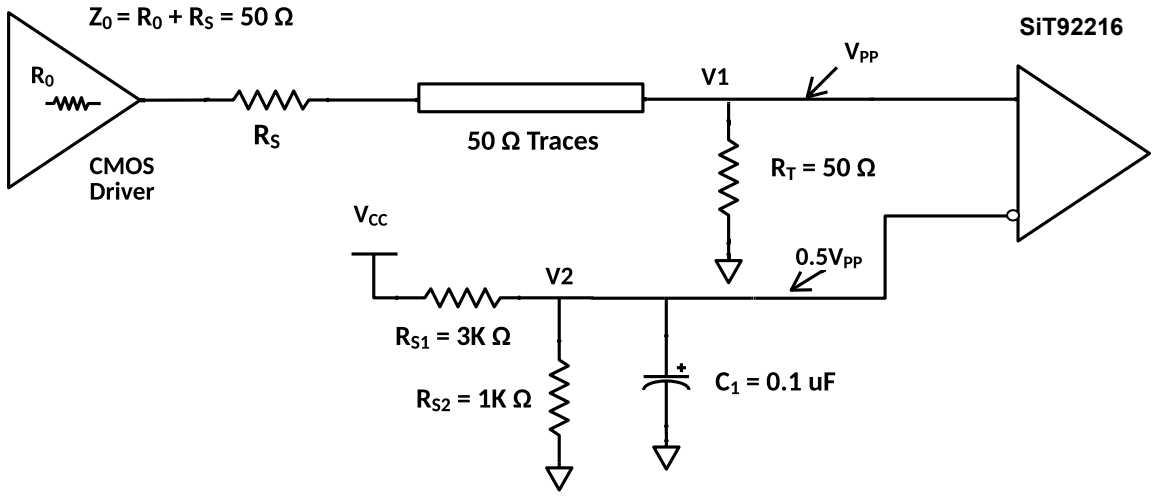


Figure 9. DC coupled LVCMOS input clock configuration – configuration 2

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 10. There is a single termination resistor RT which is connected to ground through a capacitor C_{AC}.

The value of series capacitor is given by the below formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega},$$

T_D is the transmission line delay

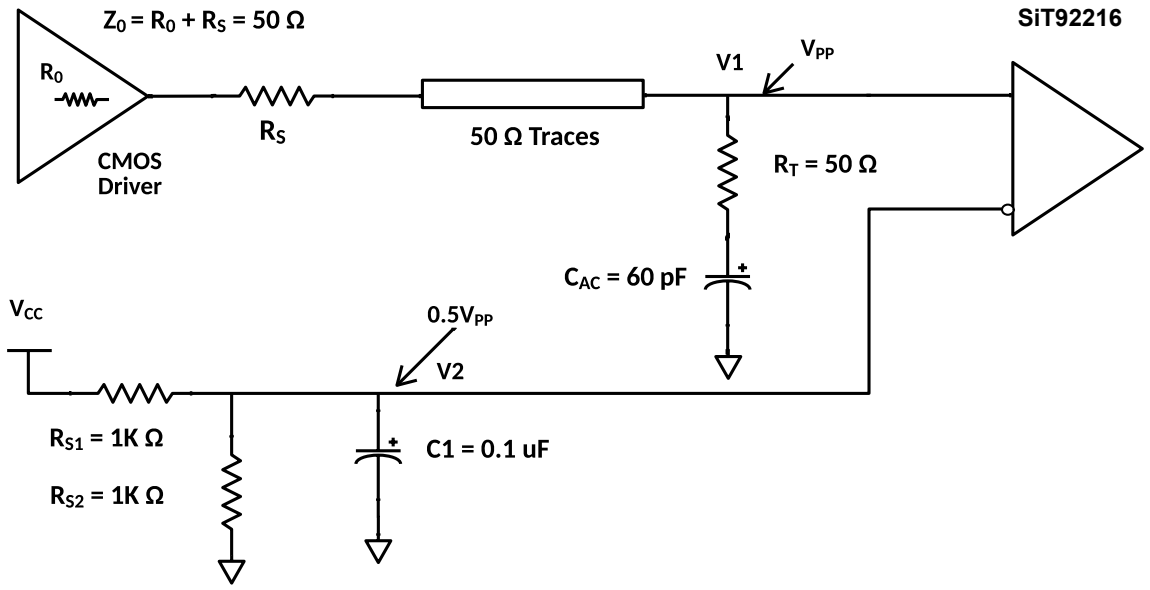


Figure 10. DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can directly couple the LVCMOS clock to SiT92216 input clock pin as shown in Figure 11.

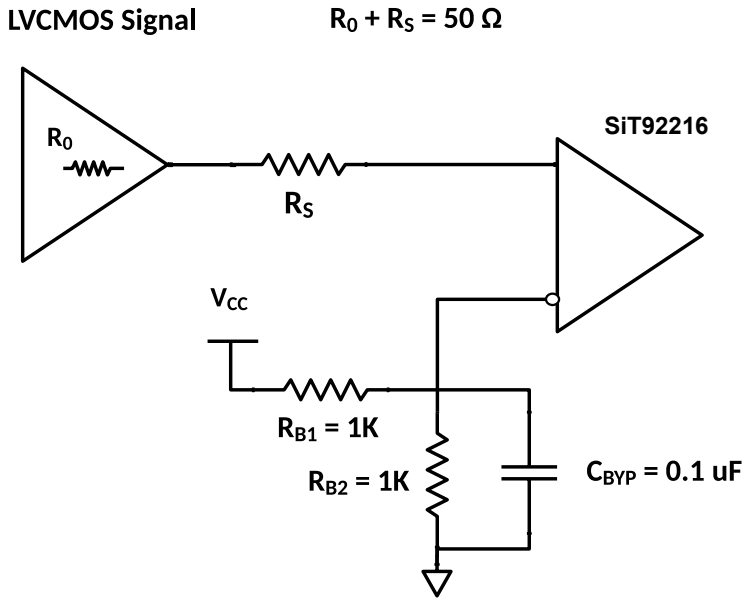


Figure 11. Direct coupling of LVCMOS clock to SiT92216

Driving OSC_IN with LVCMOS Driver (AC coupled)

The crystal input OSC_IN can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at OSC_IN should be limited to 1.5 V. The OSC_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b10. The maximum voltage at OSC_IN should not exceed 1.5 V and minimum voltage should not go below -0.3 V. The slew rate at OSC_IN should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 12 shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.65 V. The maximum DC bias voltage of OSC_IN is 0.675 V. Therefore the maximum swing at the OSC_IN pin is given by the equation given below.

$$V_{swing,pk,XTAL\_IN} = 0.675 + 0.5 * 1.65 = 1.5\ V$$

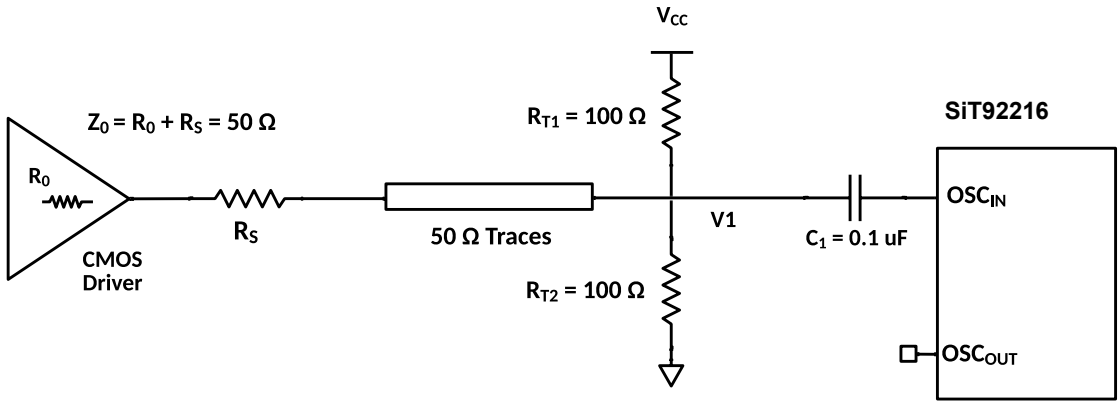


Figure 12. Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 13 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor RT to ground. A 0.1 uF is in series with the CMOS driver to prevent any DC leakage current.

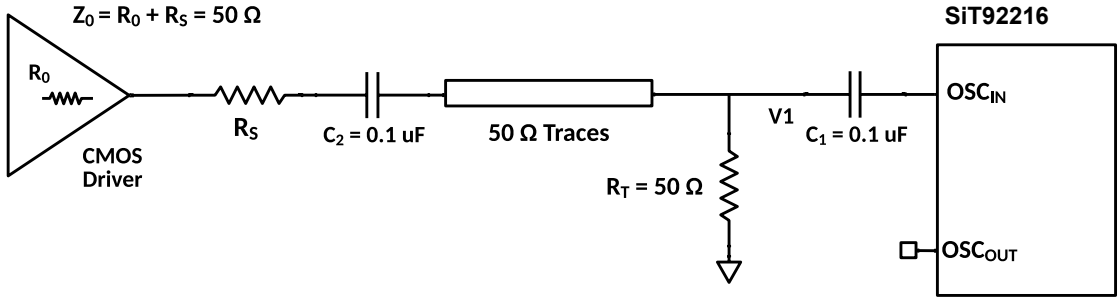


Figure 13. Single ended LVCMOS input – configuration 2, AC coupling to crystal input

Driving OSC_IN with LVCMOS Driver (DC coupled)

The crystal input OSC_IN can be overdriven with single ended clock as shown in Figure 14, in DC coupled mode. The peak swing at OSC_IN should be limited to 1.5 V (voltage at the crystal input pin). The OSC_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b11. If the LVCMOS driver is on higher supply, say 3.3 V, use a resistor divider on the PCB to scale down the peak output voltage to 1.5 V.

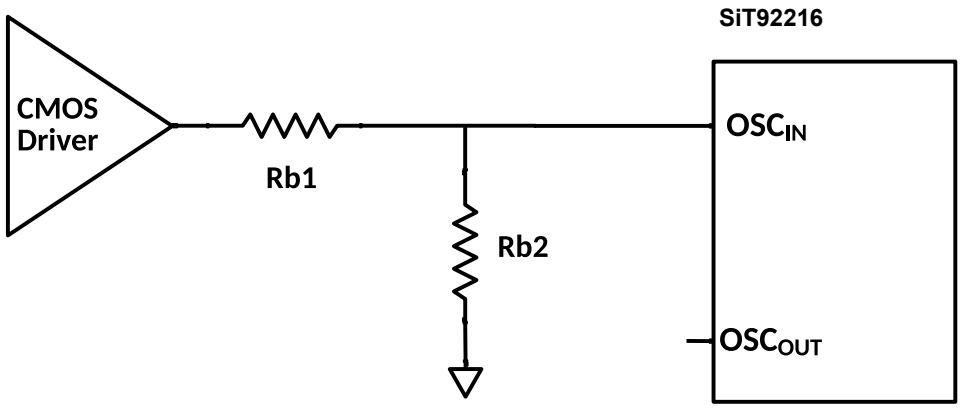


Figure 14. Single ended LVCMOS input, DC coupling to crystal input

LVDS (DC coupled)

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 15.

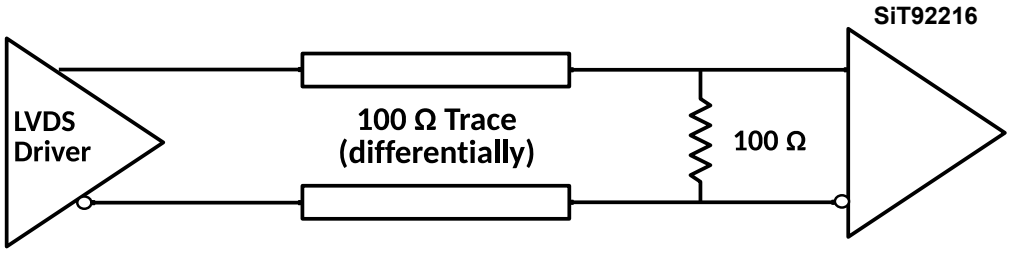


Figure 15. Termination scheme for DC coupled LVDS

HCSL (DC coupled)

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 16.

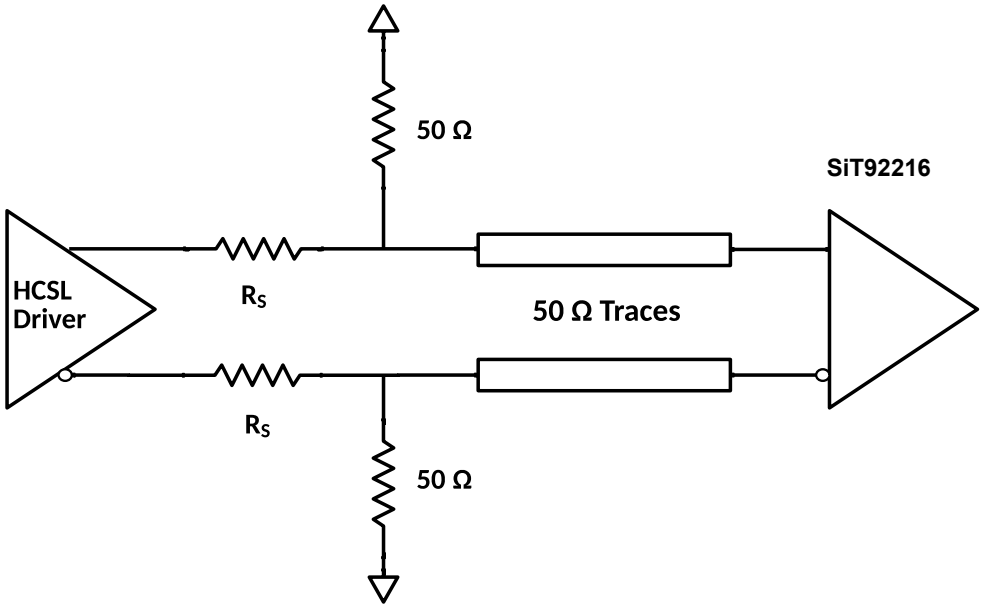


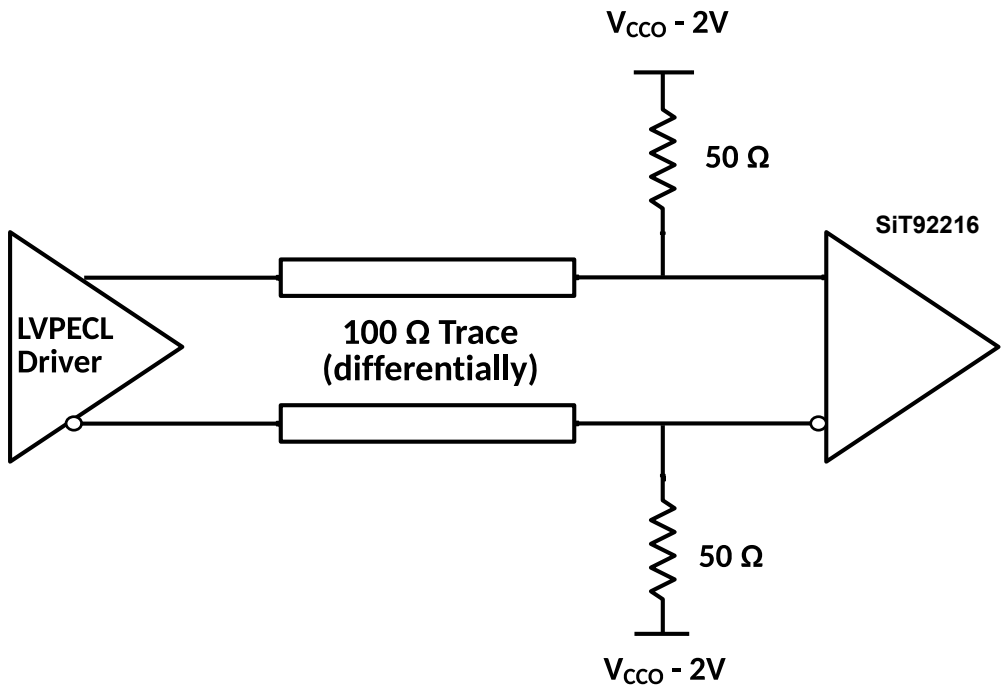
Figure 16. Termination scheme for DC coupled HCSL

LVPECL (DC coupled)

For DC coupled operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source V_{TT}.

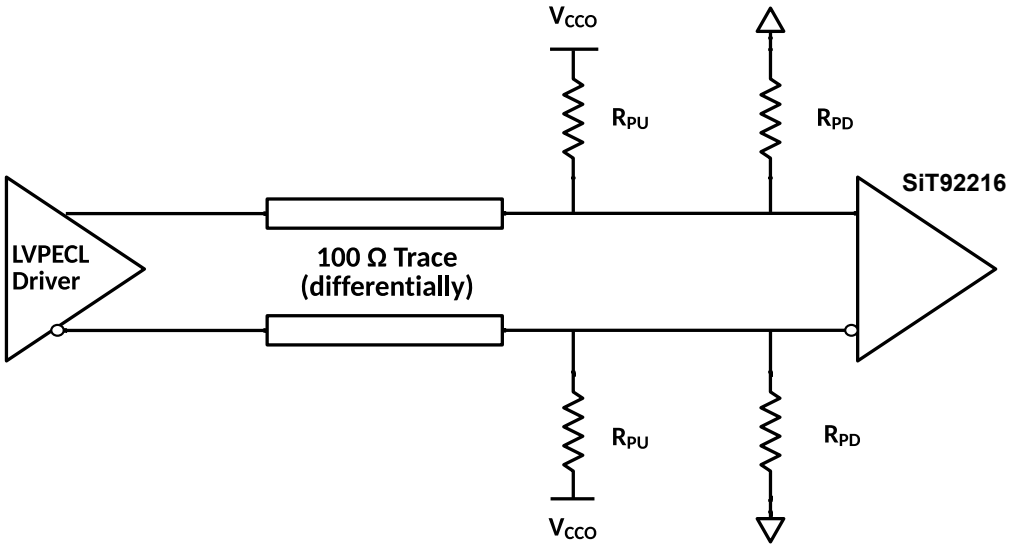
$$V_{TT} = V_{DDO} - 2V.$$

This termination scheme is shown in Figure 17, the user can also implement a Thevenin equivalent of V_{TT} using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 18.



V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 17. Termination scheme for DC coupled LVPECL



V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 18. Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * Vcco}{R_{PD} + R_{PU}} = Vcco - 2V$$

SSTL (DC coupled)

The SSTL input clock configuration is shown in Figure 19. The transmission line impedance is 60 Ω in the application example given. Therefore we use two 120 Ω resistors from V_{CCO} to ground for biasing the clock input pins. The effective termination impedance in this case is 60 Ω

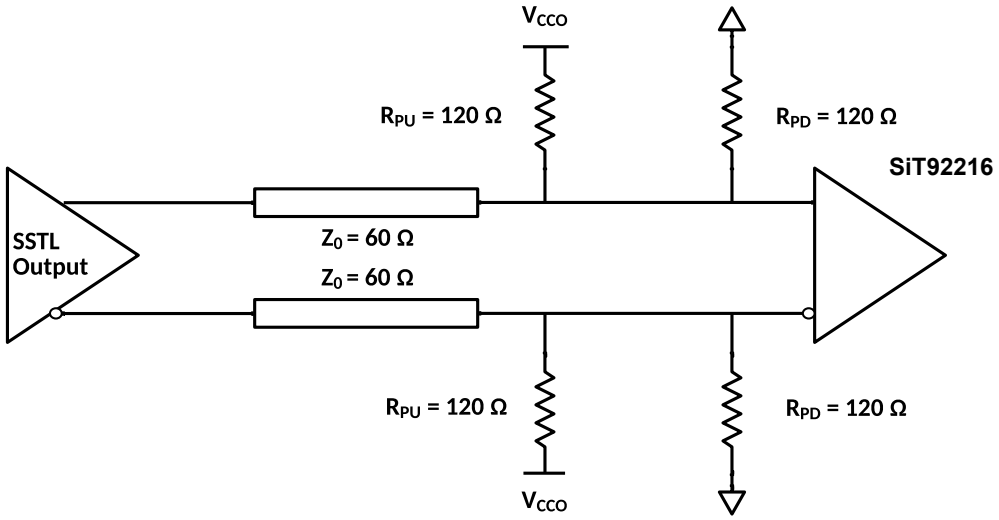


Figure 19. Example of input clock termination for SSTL clock

LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 20.

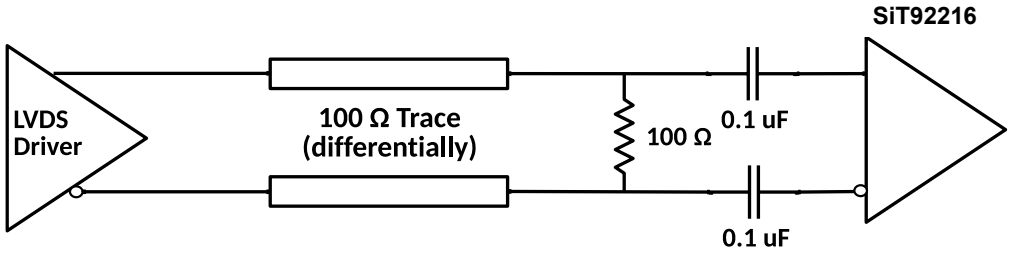


Figure 20. Termination scheme for AC coupled LVDS

LVPECL (AC coupled)

The LVPECL should have a DC path to ground. So, the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 21.

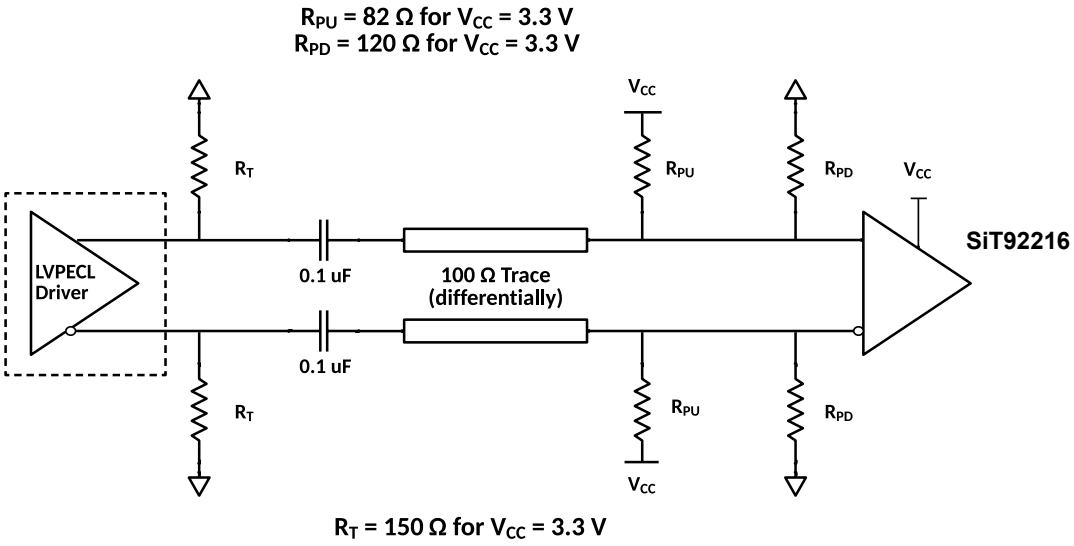


Figure 21. Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance R_{PU} and pull down resistance R_{PD} set the input common mode voltage for SiT92216.
The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{Vcc * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The differential input common mode specification of SiT92216 (from data sheet) is V_{CC} -1.1 = 2.2 V, therefore the input common mode set by LVPECL AC coupled termination meets the SiT92216 input common mode specification.

The LVPECL driver chip has resistance RT providing DC path for the output driver current in the LVPECL driver.

The effective load impedance at the input side of SiT92216 (receiver side) is formed by parallel combination of R_{PU}, R_{PD}.

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

Termination of Output Driver of SiT92216 for Various Load Configurations

SiT92216 REF_{OUT} Termination for AC Coupled mode

AC coupling of SiT92216 LVCMOS output driver is shown in Figure 22. We use single termination resistor of 50 Ω to ground. A 0.1 uF AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single 50 Ω resistance to ground. The clock signal is then AC coupled to the receiver, in this example. C1 is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50\ \Omega$$

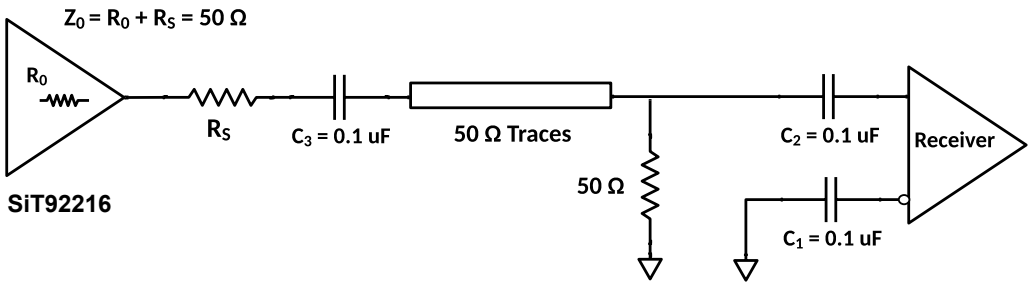


Figure 22. AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

SiT92216 REF_{OUT} Termination for DC Coupled mode

Figure 23 illustrates the termination method for the SiT92216 LVCMOS output drive, enabling clock signal transmission in DC-coupled mode. The reference voltage V1= V_{CC}/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C_1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vcc}{2},$$
$$Typical\ value\ of\ R_{s1} = R_{s2} = 1\ K\Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm,$$
$$Typical\ value\ of\ R_{T1} = R_{T2} = 100\ \Omega$$

$$\frac{Vcc * R_{T2}}{R_{T1} + R_{T2}} = \frac{Vcc}{2}$$

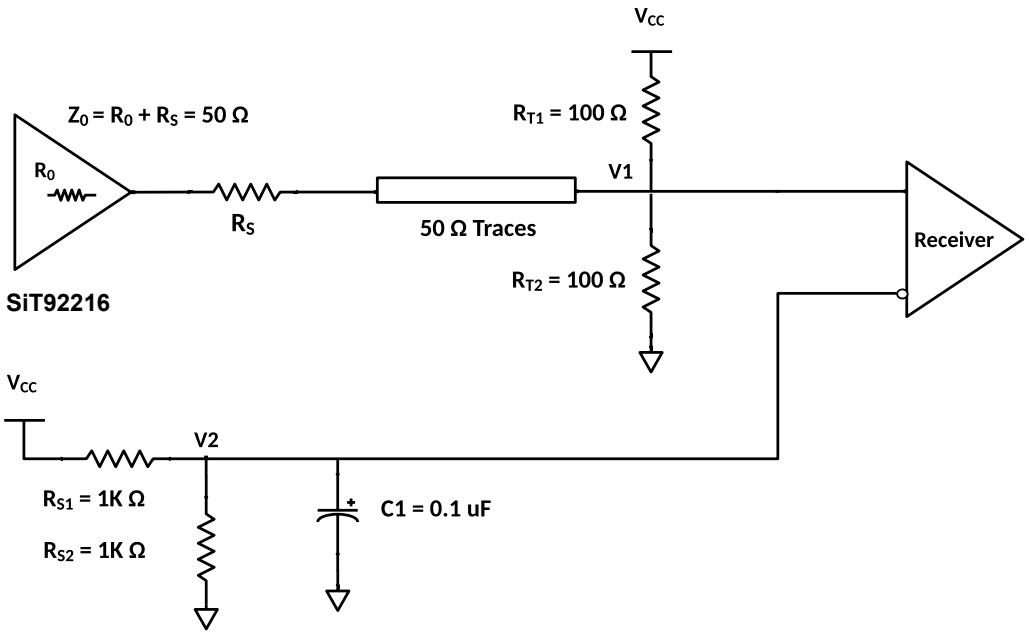


Figure 23. DC coupling of LVCMOS output clock termination – configuration 1

For example, if the SiT92216 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values below are for when both the single ended swing and V_{CC} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 24 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. There will be DC leakage current from SiT92216, for the output termination shown in Figure 24. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 24 is given below.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{Vcc * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2} = \frac{Vcc}{4}, Typical\ value\ of\ R_{s1} = 3K\Omega, R_{s2} = 1\ K\Omega$$

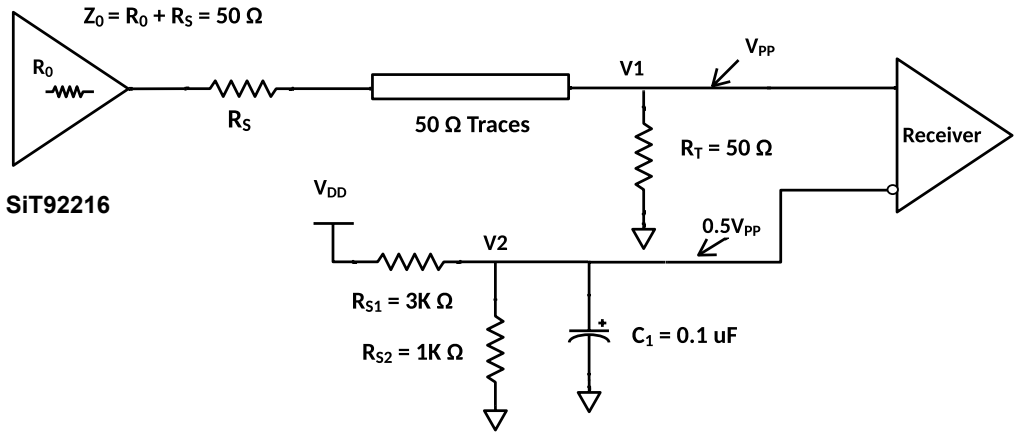


Figure 24. DC coupled LVCMOS output clock configuration – configuration 2

The SiT92216 LVCMOS output driver termination with series RC termination near the buffer is shown in Figure 25. There is a single termination resistor RT which is connected to ground through a capacitor CAC.

The value of series capacitor is given by the below formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega},$$

T_D is the transmission line delay

Typical value for C_{AC} is 60 pF, assuming delay of T_D = 200 ps/inch and 5 inch input clock route length.

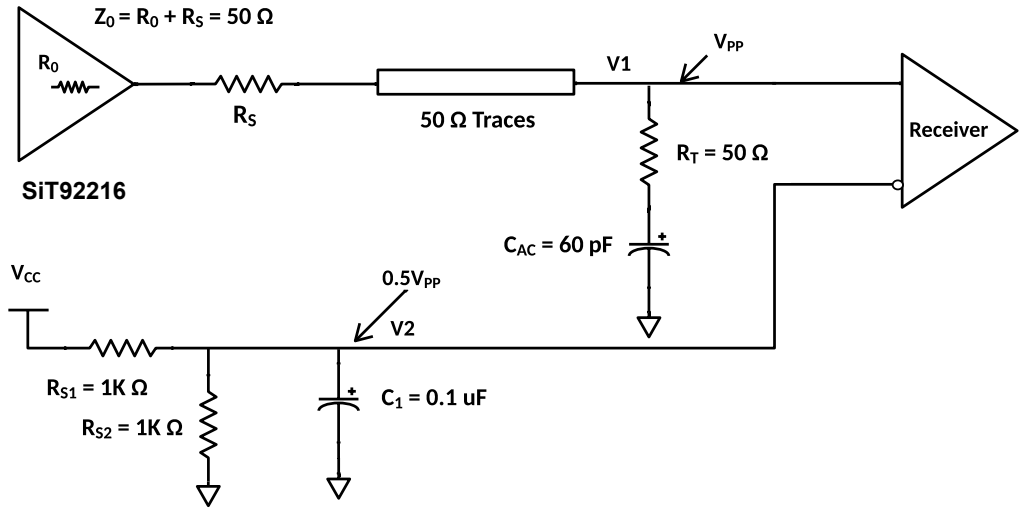


Figure 25. DC coupled LVCMOS output clock with series RC termination – configuration 3

The typical value of R_{S1} and R_{S2} in this case is 1K Ω and that of C_{AC} is 60 pF.

CMOS (Capacitive load)

The capacitive load can be driven as shown in Figure 26. For SiT92216 LVCMOS driver the R_O is very close to 50 Ω by design. Therefore R_S = 0 Ω is recommended.

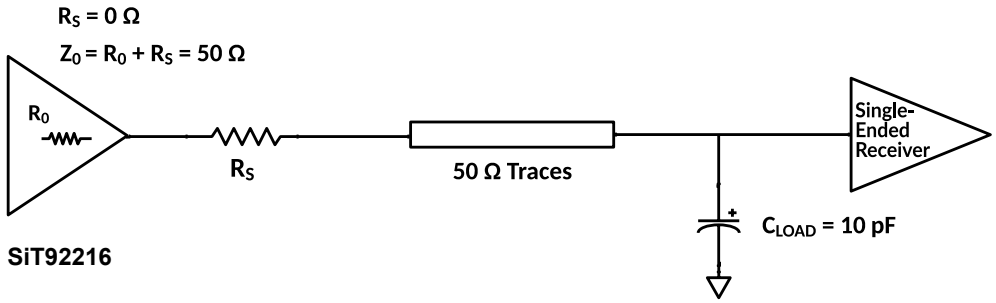


Figure 26. Typical application load

Termination of Output Drivers (DC coupled)

LVDS DC Coupled Output Termination

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 27.

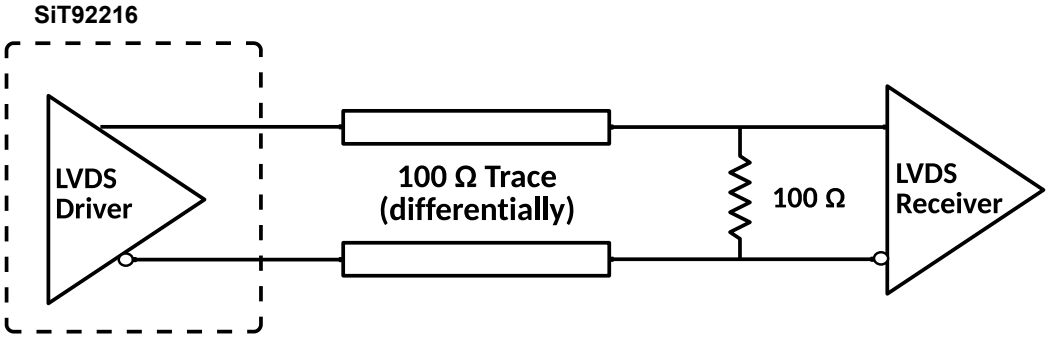


Figure 27. Termination scheme for DC coupled LVDS

HCSL DC Coupled Output Termination

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 28.

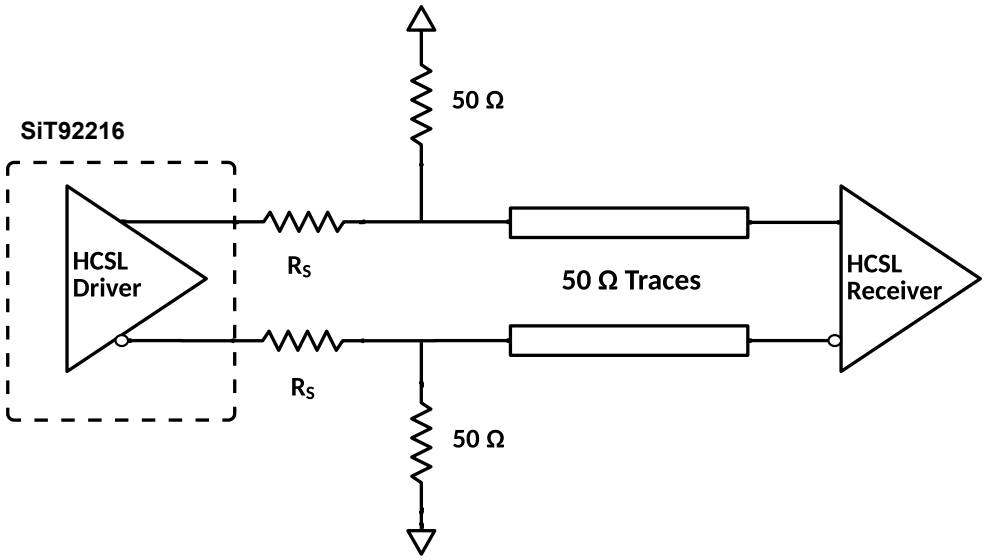
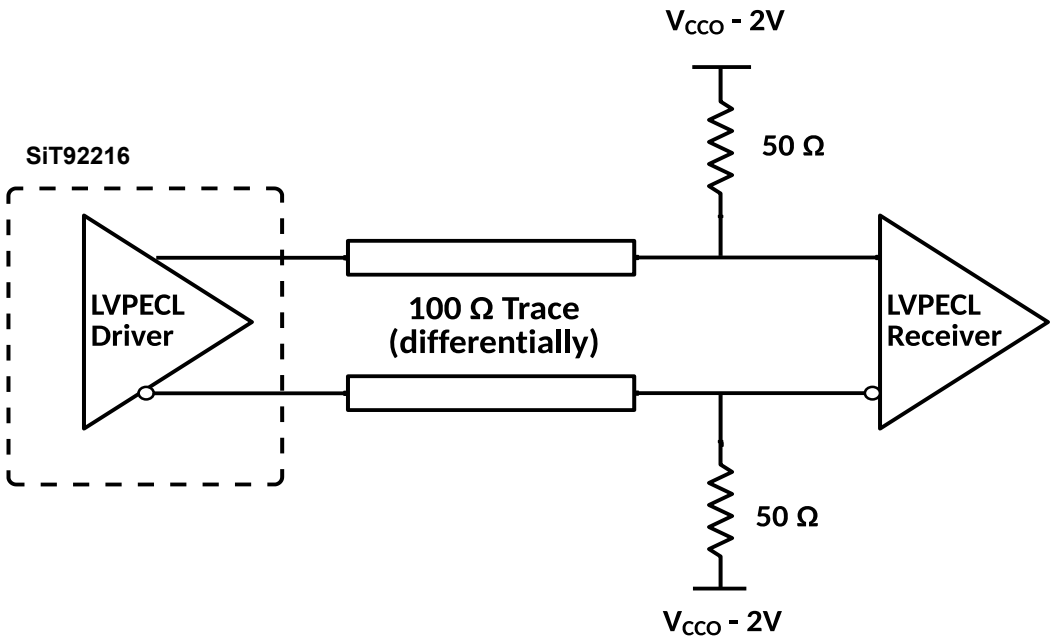


Figure 28. Termination scheme for DC coupled HCSL

LVPECL DC Coupled Output Termination

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source V_{TT}. Typically, $\boldsymbol{V_{TT} = V_{CCO} - 2V}$. This termination scheme is shown in Figure 29.



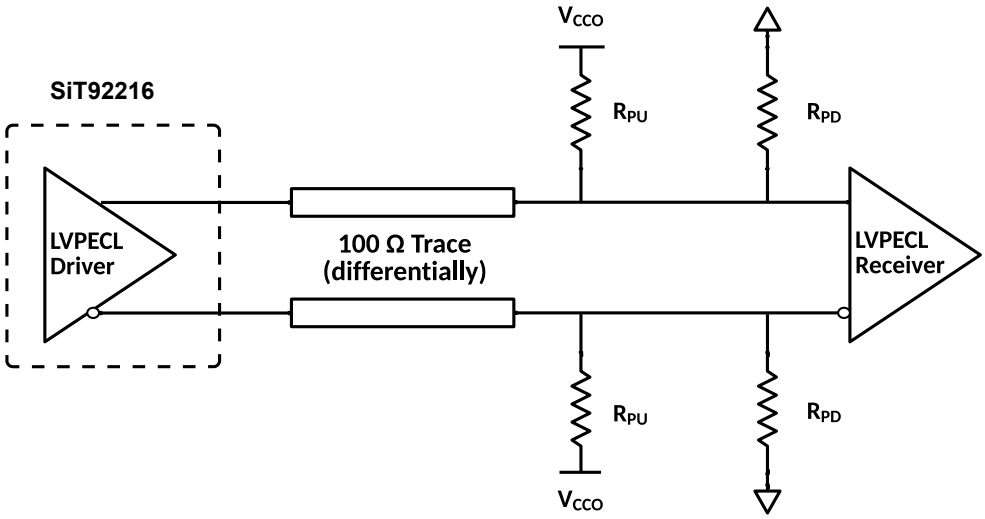
VCCO	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 29. Termination scheme for DC coupled LVPECL

Alternatively, the user can also implement a Thevenin equivalent of VTT using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 30.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * Vcco}{R_{PD} + R_{PU}} = Vcco - 2V$$



V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 30. Termination scheme for DC coupled LVPECL, Thevenin equivalent

Termination of Output Drivers (AC coupled)

LVDS AC Coupled Output Termination

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 31.

First figure shows SiT92216 output driver configured in LVDS mode. The receiver in this case is shown as LVDS receiver. The second figure shows SiT92216 output driver configured in LVDS mode and the receiver in this case is shown as CML receiver. If the LVDS swing is compatible with the receiver, the AC-coupled output termination remains unchanged.

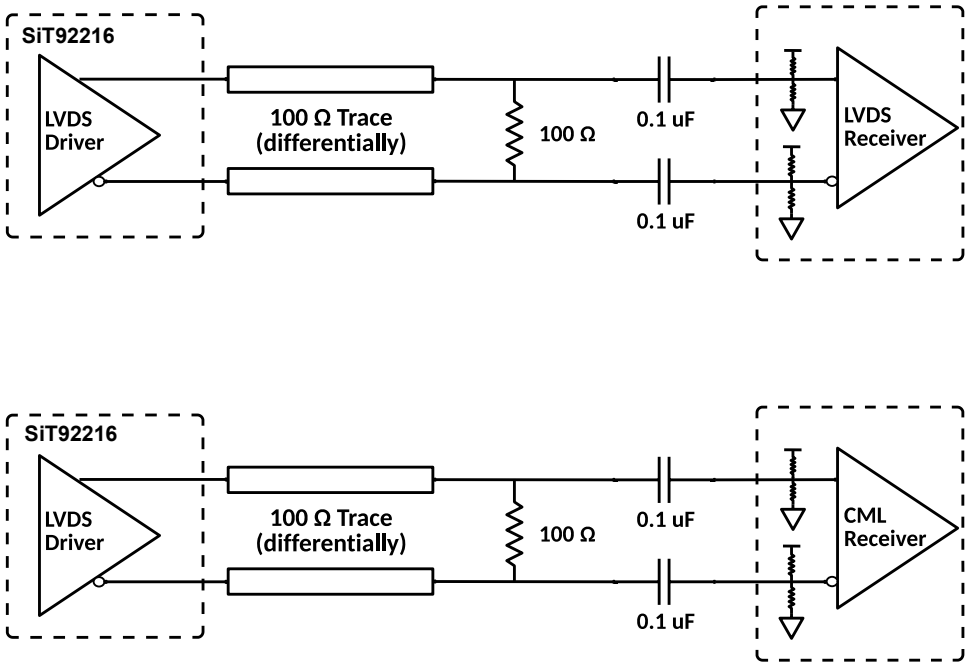


Figure 31. Termination scheme for AC coupled LVDS, driving LVDS receiver and CML receiver

LVPECL AC Coupled Output Termination

The LVPECL should have a DC path to ground. So the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 32. SiT92216's swing reduces by about 20% as the effective load resistor is now the parallel combination of RT at the driver side and 50 Ω at the receiver side.

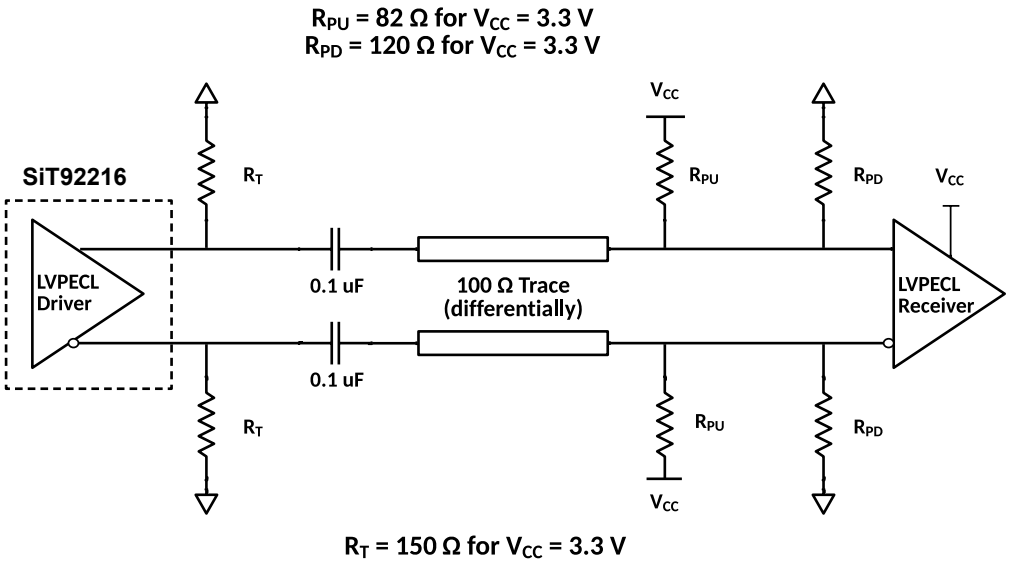


Figure 32. Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance R_{PU} and pull down resistance R_{PD} sets the input common mode voltage for LVPECL receiver. The value of the input common mode voltage can be estimated by the equation given below

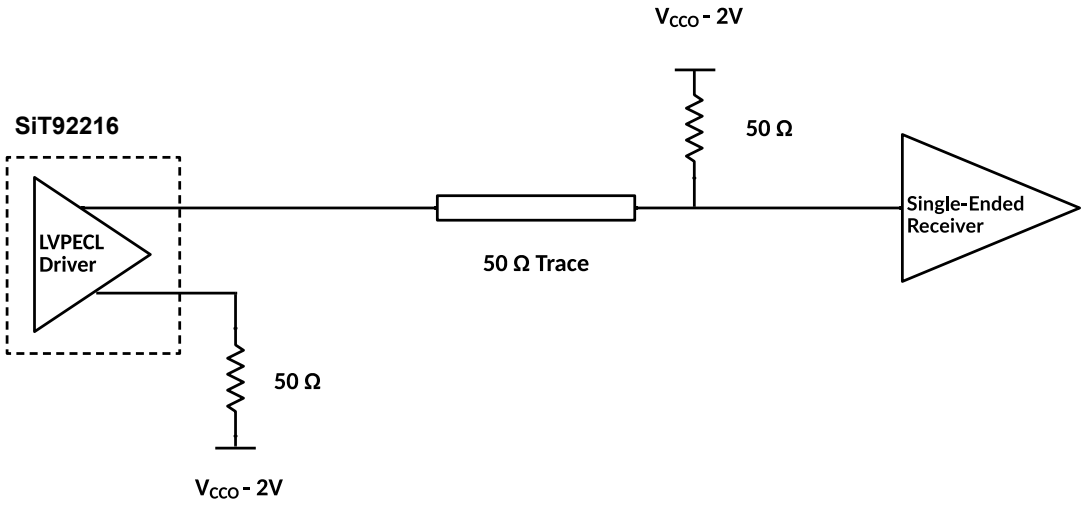
$$V_{ICM} = \frac{Vcc * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The LVPECL driver of SiT92216 has resistance RT providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the receiver side is formed by parallel combination of R_{PU}, R_{PD}. The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

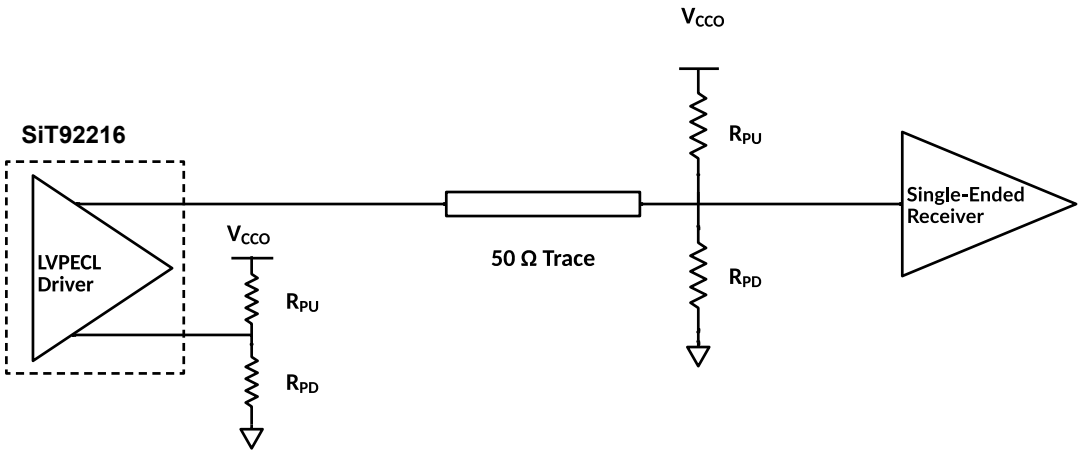
Termination of Output Drivers in LVPECL Mode, Single Ended, DC coupled

It is possible to implement Single ended LVPECL interface. The user can use a balun to convert differential output to single ended output. It is also possible to use the LVPECL driver as one or two separate 700 mV - PP signals. The unused output needs to be terminated close to the output driver. These termination schemes are shown in Figure 33 and Figure 34.



V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 33. Termination scheme for DC coupled LVPECL, single ended



V_{CCO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 34. Termination scheme for DC coupled LVPECL, single ended, Thevenin equivalent

Termination of Output Drivers in LVPECL Mode, Single Ended, AC coupled

LVPECL output driver needs a DC path to ground from its output. Therefore 160 Ω (if V_{CC} = 3.3 V) resistor to ground is connected from the output of the LVPECL driver to ground. If V_{CC} = 2.5 V, the DC path resistance should be 91 Ω. The 50 Ω load termination resistor must be placed close to input receiver and biased to a suitable voltage.

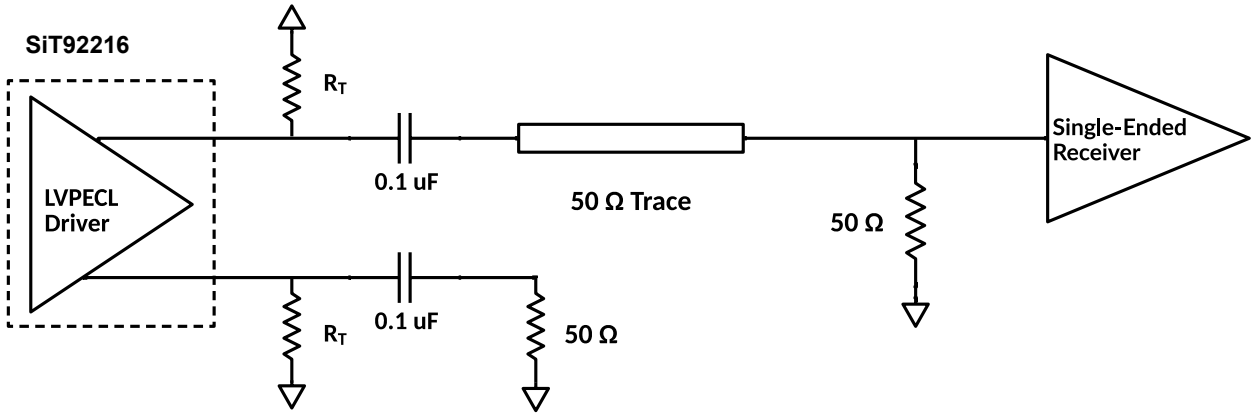


Figure 35. Termination scheme for AC coupled LVPECL, single ended

Termination of Output Drivers in AC coupled HCSL mode

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. AC coupling capacitor of 0.1 uF is used to couple the output HCSL signal in to the receiver. The same termination can be used for CML receiver.

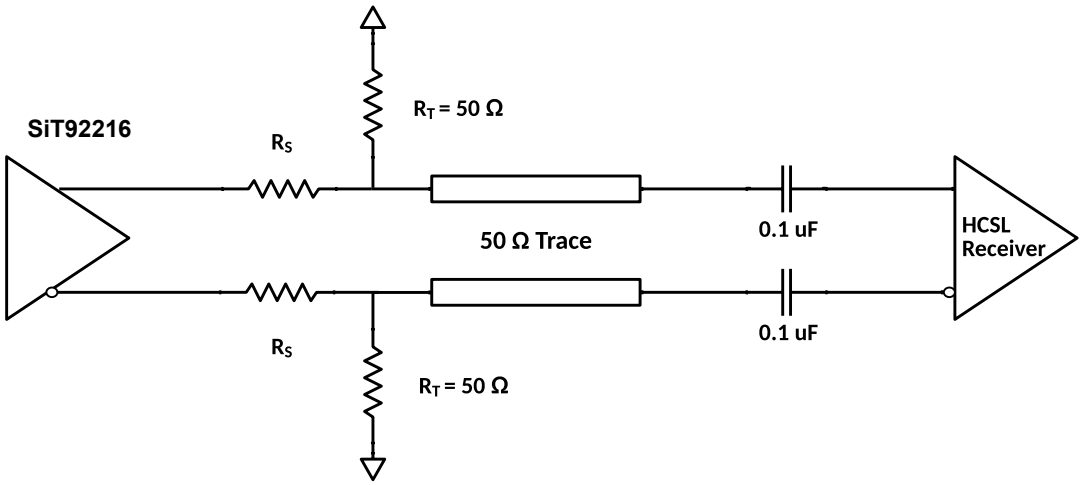


Figure 36. Output driver termination in HCSL AC coupled mode

Hot Swap Recommendations

Introduction

Hot-swap is a term used to refer to the insertion and removal of a daughter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can get damaged.

Typical Differential Input Clock

For example, Figure 37 shows a typical LVPECL driver and differential input. If the power of the driver (V_{CCO}) is turned on before the input supply (V_{CCI}), there is a possibility that the input current could exceed the limit and damage diode D1.

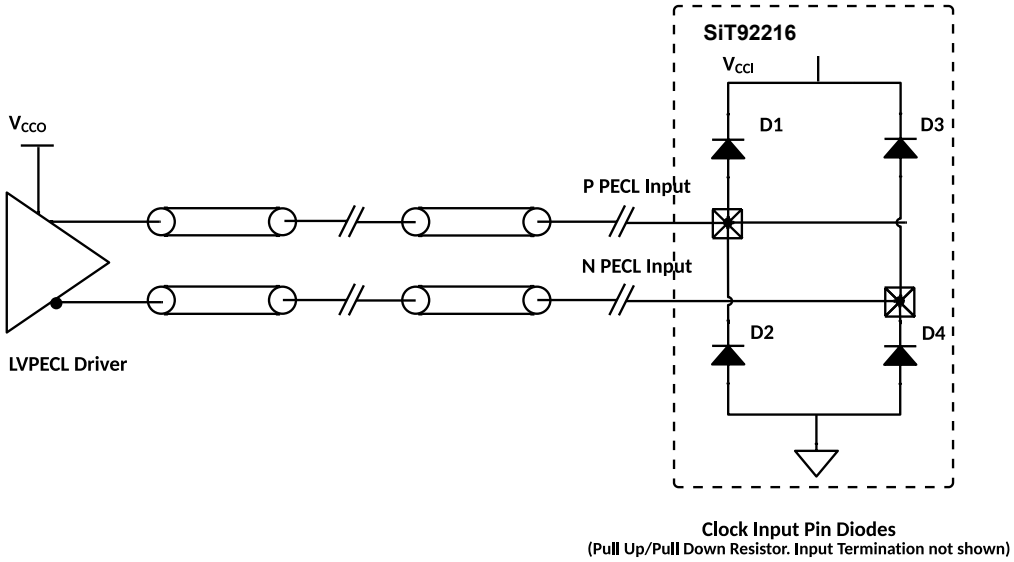


Figure 37. Typical input differential clock

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though it's not necessary, but if board space allows, some of the examples have an optional 100 pF capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible.

Input Clock Termination with Hot Swap Protection

LVPECL Termination Example

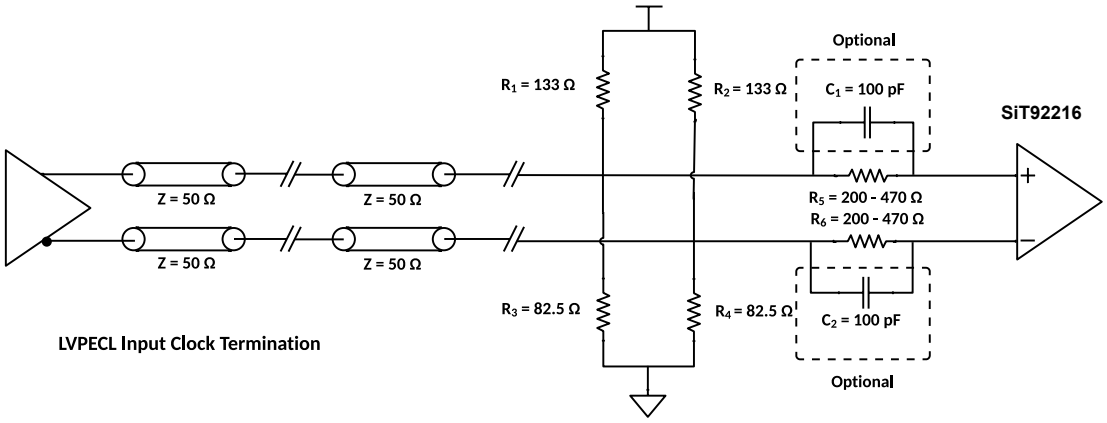


Figure 38. LVPECL termination with hot swap protection

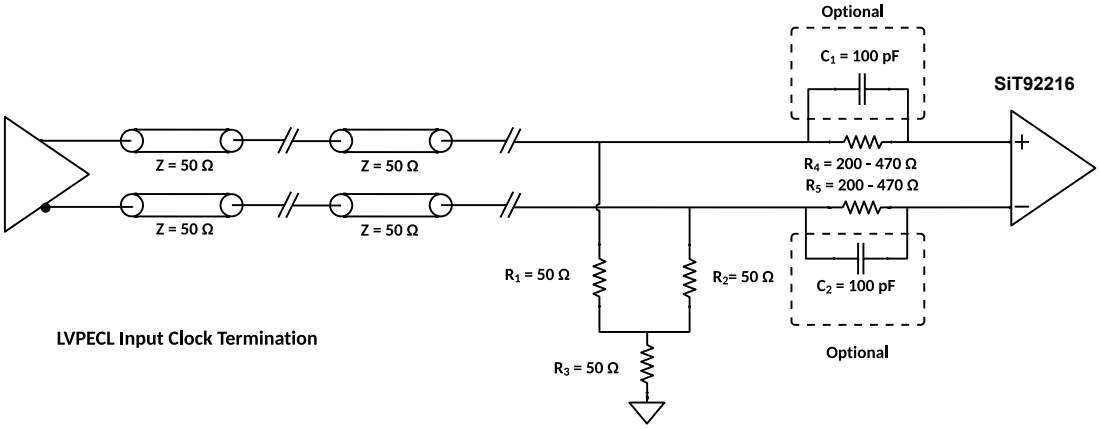


Figure 39. LVEPCL termination with hot swap protection

LVDS Input Clock Termination Example

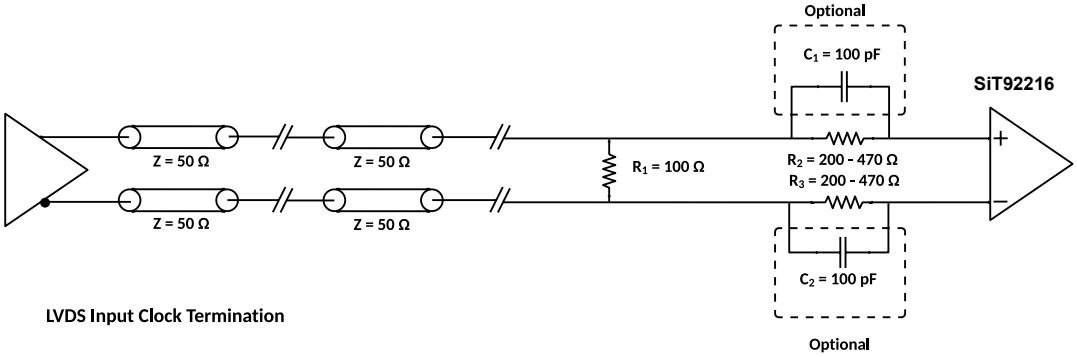


Figure 40. LVDS termination with hot swap protection

HCSL Input Clock Termination Example

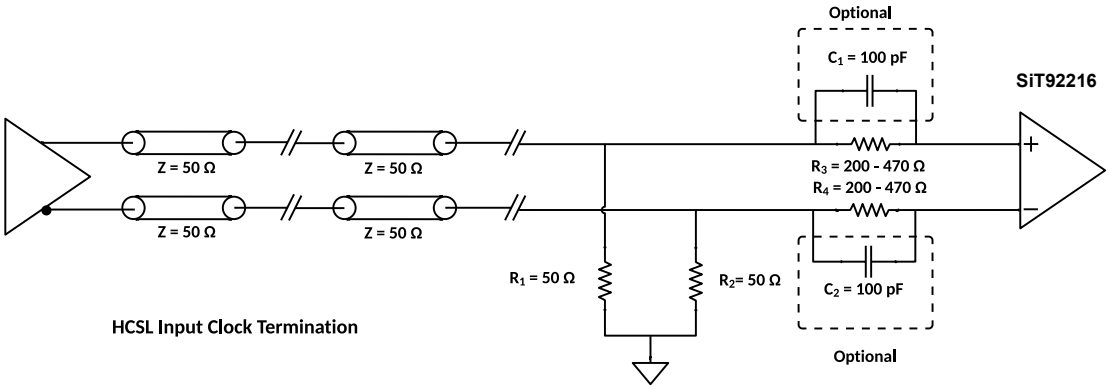


Figure 41. HCSL termination with hot swap protection

LVCMOS Input Clock Termination with Hot Swap Protection

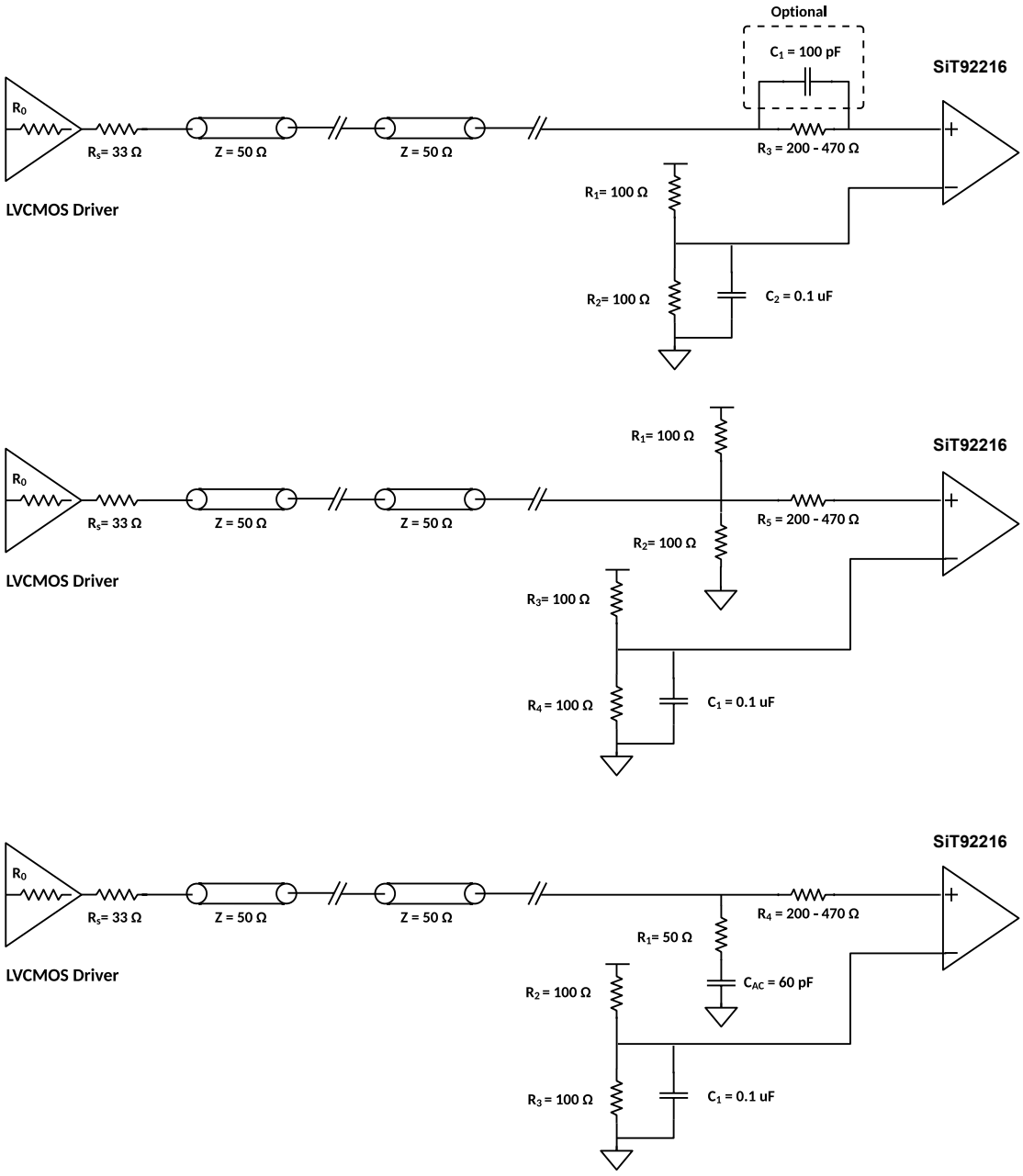


Figure 42. LVCMOS input clock termination with hot swap protection

LVCMOS Output Clock Termination with Hot Swap Protection

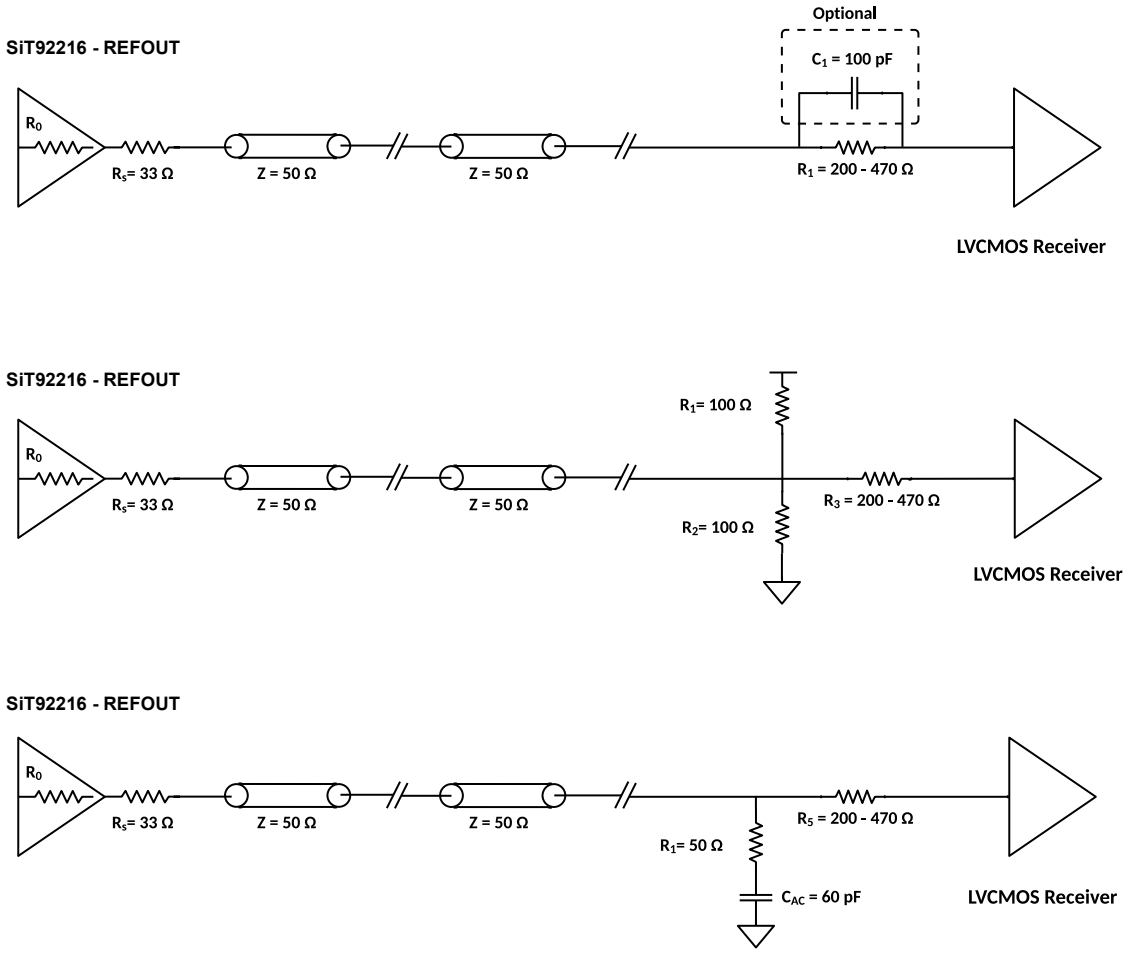


Figure 43. Different types of LVCMOS output clock termination with hot swap protection

Parameter Measurement Information

Differential Input Level

The parameter definitions related to differential input level are shown in Figure 44.

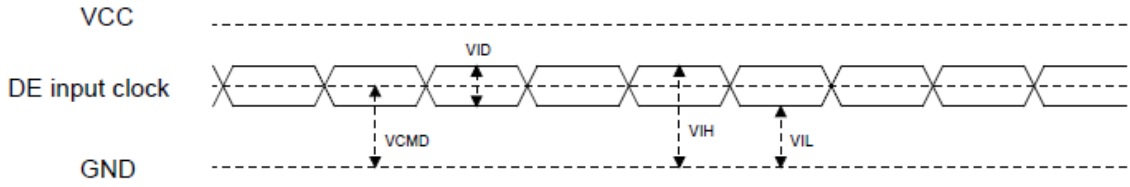


Figure 44. Parameters related to differential input level

Differential Output Level

The parameter definitions related to differential output level are shown in Figure 45.

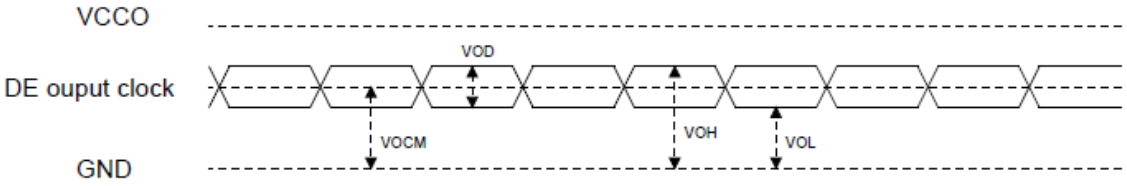


Figure 45. Parameters related to differential output clock levels

Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown in Figure 46.

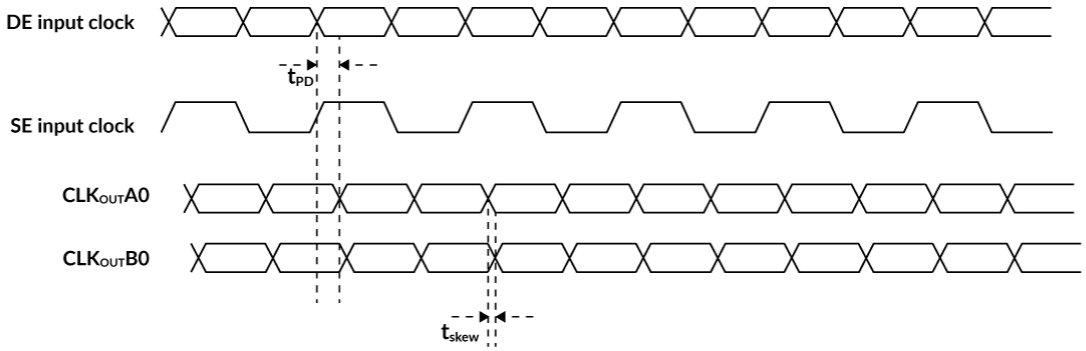


Figure 46. Parameter definitions of propagation delay and skew

Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown in Figure 47.

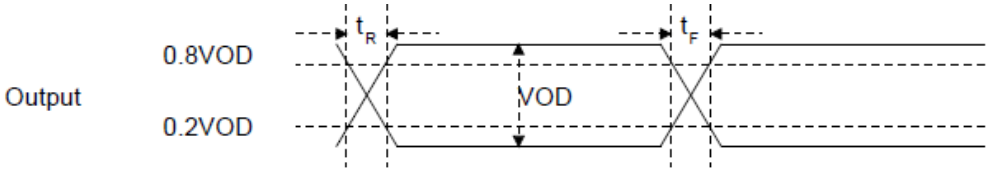


Figure 47. Parameter definitions related to rise and fall times

Isolation

Isolation measures how much toggling in an unused clock input influences the output clock. Let us say that Clock0 path is selected and there the clock frequency is 156.5 MHz at 0 dBm power. If a clock is toggling in Clock1 path at 156 MHz at 0 dBm, then there may be a tone at an offset of 0.5 MHz from the carrier, in the output clock. The power of this tone with respect to the carrier is called isolation.

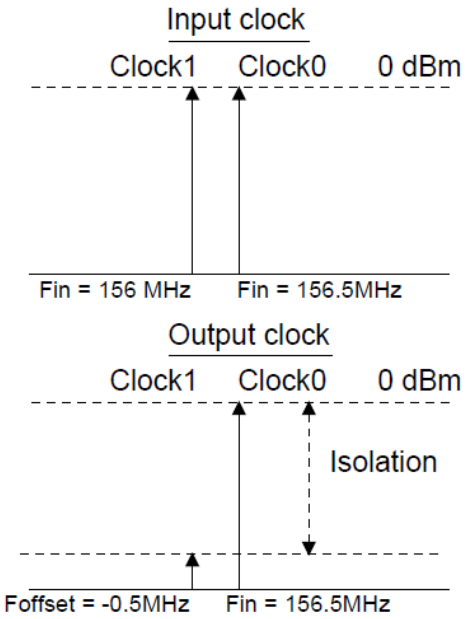


Figure 48. Parameter definition of isolation

Operation in Multiple VCCO Supply Domains

The V_{CCOA} pins, 2 and 5 on the left side are shorted internally. These pins along with ODR $CLK_{OUT}A0$ and $CLK_{OUT}A1$ belong to a single supply domain. The V_{CCOB} pins, 20 and 23 on the right side are shorted internally. These pins along with ODR $CLK_{OUT}B0$ and $CLK_{OUT}B1$ belong to a single supply domain. These two supply domains are totally independent of each other. Pins 2 and 5 can be connected to say 3.3 V while Pins 20 and 23 can be connected to 2.5 V. In this example, $CLK_{OUT}A0$ and $CLK_{OUT}A1$ will be 3.3 V output driver. $CLK_{OUT}B0$ and $CLK_{OUT}B1$ will be 2.5 V output driver.

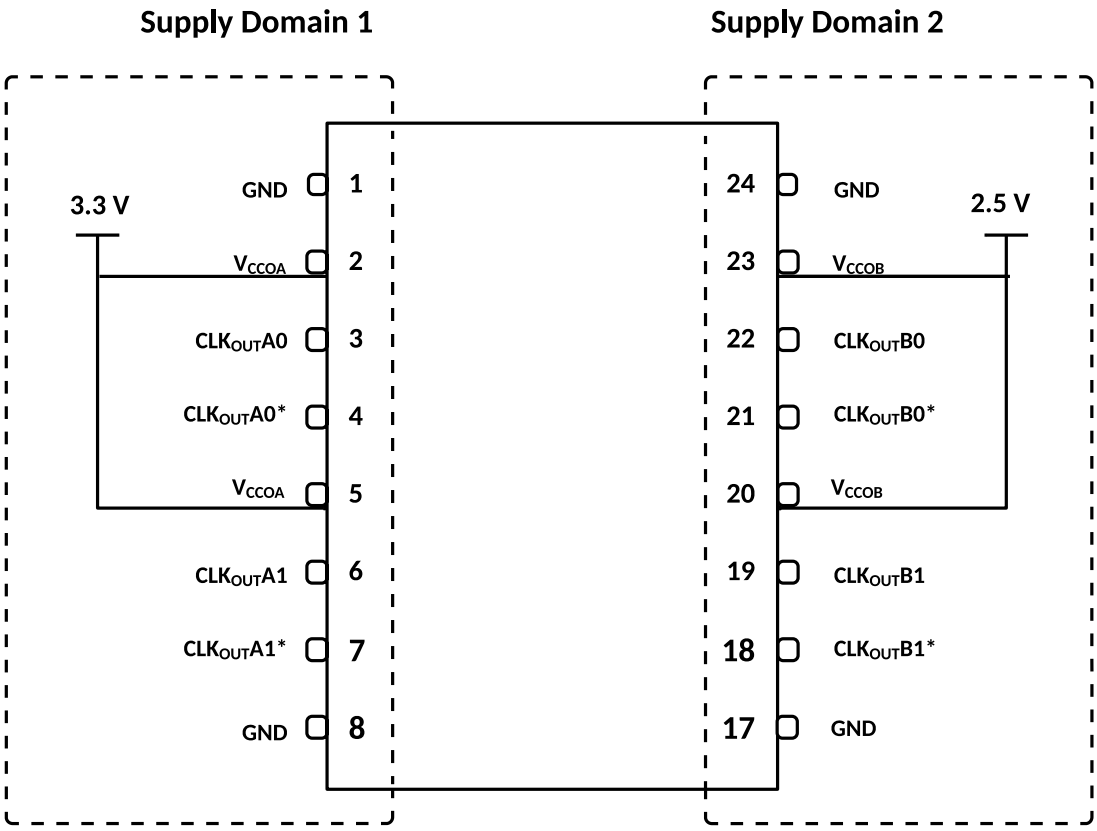
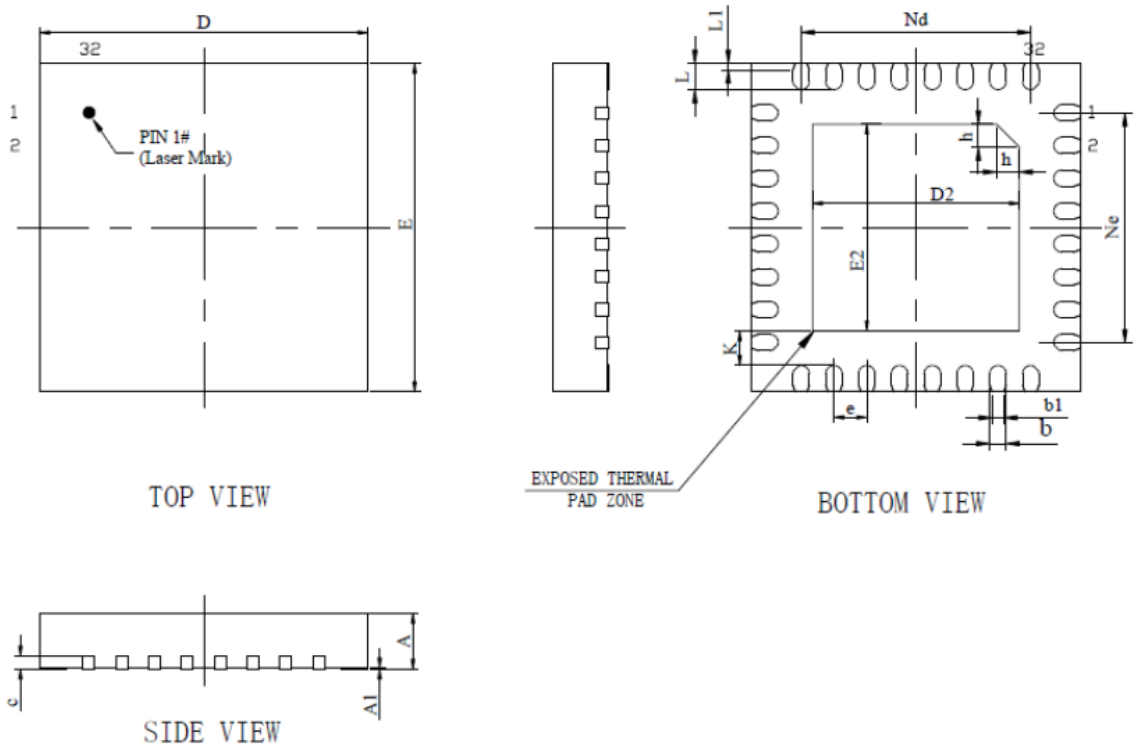


Figure 49. Multi Supply operation of SiT92216

Package Dimensions and patterns

Package Dimension (in mm)[1,2,3]



SiT92216 32-pin 5 mm x 5mm Package Diagram

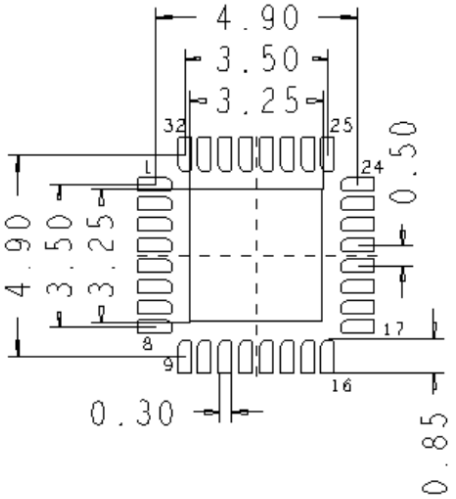
Notes:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c		0.203 REF	
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
e		0.50 BSC	
Nd		3.50 BSC	
Ne		3.50 BSC	
E	4.90	5.00	5.10
E2	3.05	3.15	3.25
L	0.35	0.40	0.45
L1		0.10 REF	
h	0.30	0.35	0.40
K		0.525 REF	

Land pattern

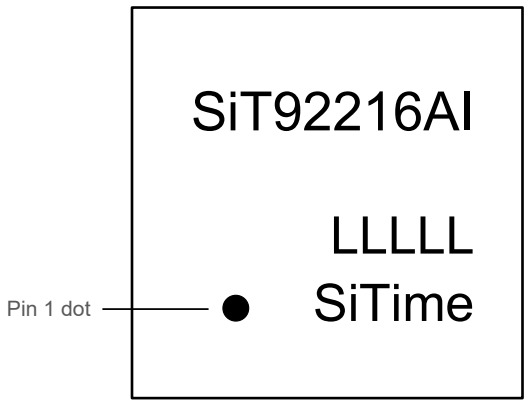
Land Pattern (Unit: mm) [1,2]



Notes:

1. All dimensions shows are in millimeters (mm) unless otherwise indicated.
2. Land patter n design is based on IPC-7351 guidelines.

Top Marking



Line 1: “SiT92216AI”, SiTime part number
Line 2: Blank
Line 3: “LLLLL”, Lot code from SiTime
Line 4: Pin 1 dot and “SiTime” logo

Revision History

Table 21. Revision History

Revisions	Release Date	Change Summary
0.5	10-Nov-2023	Initial Release
0.51	8-Jul-2024	Ordering Information update
0.52	31-Jan-2025	Ordering Code for Packaging updated with 4Ku/reel code “P” Added Top Marking section
0.53	28-Mar-2025	Ordering Code for Packaging updated with 4Ku/reel code “P” and 500u/reel code “N”
1.0	18-Aug-2025	Production Release
1.1	5-Jan-2026	Updated PCIE Gen6 Jitter and Land Pattern
1.2	22-Jun-2026	Updated max specs for additive jitter and output skew Updated PCIE Gen7 support Updated disclaimer
1.3	17-Oct-2026	LVDS output differential peak voltage conditions and specs updated

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