

SiT92208

8 Output, Differential, Ultra Low Jitter Buffer



Description

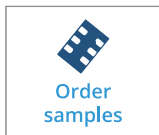
The SiT92208 is a 2.1 GHz, 8 output low-jitter clock fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution and level translation.

The buffer can choose a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock can be distributed to two output drive banks A, B and one LVCMOS output.

The crystal input can support crystals from 8 MHz to 50 MHz. It can also support single ended clock.

The output drivers of each bank can be independently programmed to LVPECL, LVDS, HCSL or HIZ mode. The LVCMOS clock output is synchronized to selected clock and can be enabled or disabled in a glitch free manner.

The SiT92208 operates from a 3.3 V/2.5 V core supply and 3 independent 3.3 V/2.5 V/1.8 V output supplies. LVCMOS output driver can be operated at 1.8 V.



Features

- Additive jitter performance of 55 fs RMS
- 3:1 input clock selection
- Two universal clock inputs can operate up to 2.1 GHz and accept LVPECL, LVDS, LVCMOS, CML(ac-coupled only), HCSL, SSTL or single ended clocks
- One crystal input which can support crystals in the frequency range of 8 MHz to 50 MHz or it can accept single ended input clock.
- Two output driver banks A and B which can be programmed independently to LVPECL, LVDS, HCSL or HIZ mode.
- Output skew between clock outputs < 60 ps
- Level translation with core supply voltage of 3.3 V/2.5 V and 3.3 V/2.5 V output supply for differential output drivers.
- 3.3 V/2.5 V/1.8 V operation for the single LVCMOS output driver and HCSL Driver
- The SiT92208 buffer is pin controlled.
- High PSRR -70/-73 dBc for LVPECL/LVDS modes
- SiT92208 buffer is available in a 40-pin, 6 mm x 6 mm QFN package
- Support PCI-e Gen1 to Gen7

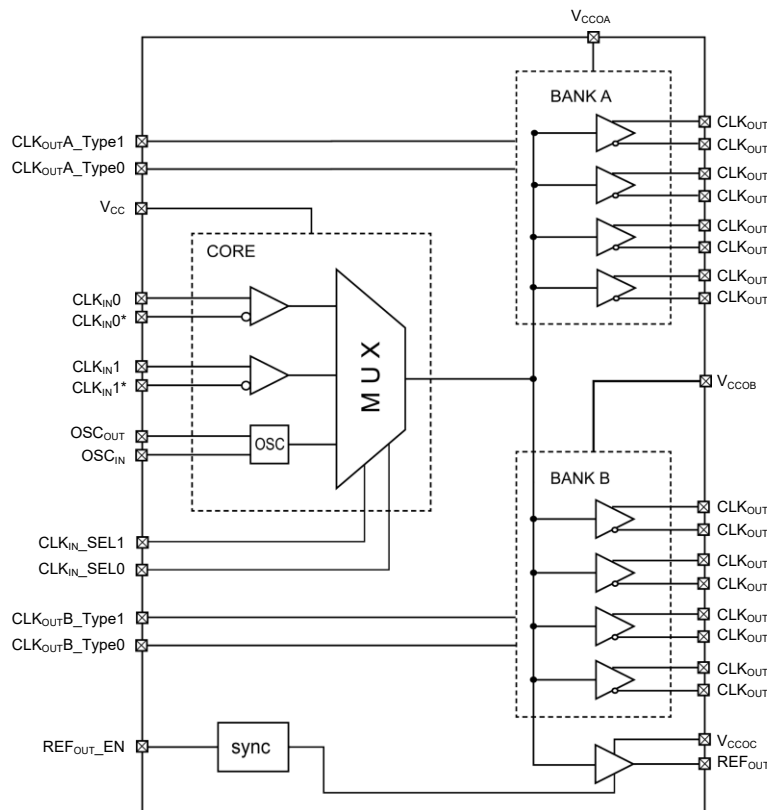
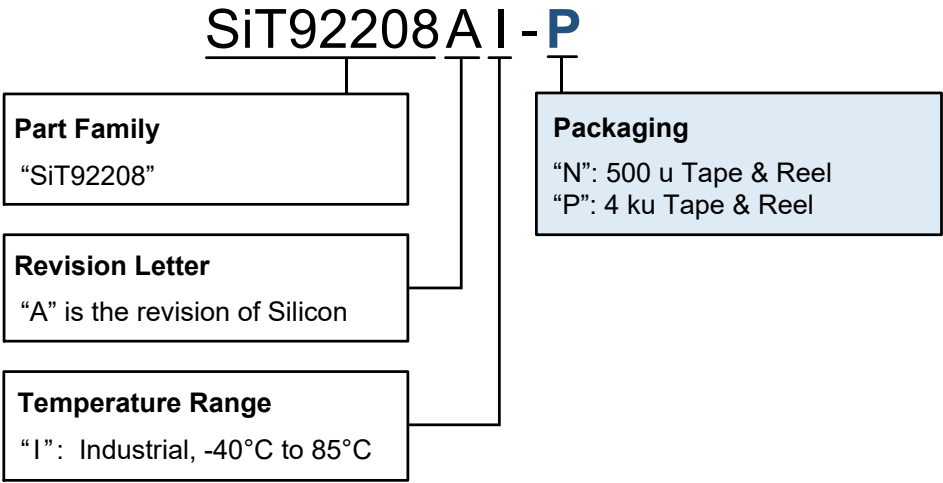


Figure 1. SiT92208 Block Diagram

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Ordering Information



Electrical Characteristics

Table 1. Absolute Maximum Ratings ^[1,2]

Parameters	Symbol	Min	Typ	Max	Units
Core supply voltage, Analog Input	V _{CC}	-0.3		3.6	V
Output bank supply voltage	V _{CCO}	-0.3		3.6	V
Input voltage, All Inputs, except OSC _{IN}	V _{IN}	-0.3		3.6	V
OSC _{IN}	V _{IN}	-0.5		1.8	V
Storage temperature	T _S	-55		150	°C
Moisture Saturation Level	MSL		3		

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Units
Core Supply Voltage	V _{CC}	3.135	3.3	3.45	V
	V _{CC}	2.375	2.5	2.625	V
Output Supply Voltage	V _{CCOA/B}	3.135	3.3	3.45	V
	V _{CCOA/B}	2.375	2.5	2.625	V
	V _{CCOA/B} ¹	1.71	1.8	1.89	V
Output Supply Voltage for LVCMOS Driver	V _{CCOC}	3.135	3.3	3.45	V
		2.375	2.5	2.625	V
		1.71	1.8	1.89	V
Ambient Temperature	T _A	-40		85	°C
Junction Temperature	T _J			125	°C

Note:

- Only for HCSSL

Table 3. Electrical Characteristics

Unless otherwise specified: V_{CC} = 3.3 V ±5%, 2.5 V ±5%, V_{CCO} = 3.3 V ±5%, 2.5 V ±5%, -40°C ≤ T_A ≤ 85°C, CLK_{IN}0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, V_{CCO} = 3.3 V, T_A = 25°C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Current Consumption						
Core Supply Current when Input Buffer is selected	CLKIN0/1 selected, V _{CC} = 3.3 V/2.5 V ± 5%, V _{CC} = V _{CCO}	I _{CC_CORE}		16.5	19.8	mA
Core Supply Current when Crystal is selected	XO selected, V _{CC} = 3.3 V/2.5 V ± 5%, V _{CC} = V _{CCO}	I _{CORE_XO} ^[4]			14	mA
Increment in Core Supply when all ODR Banks are enabled		I _{CC_ODR_EN}			2	mA
Frequency Dependent Current both banks on Core Supply. This Current scales with Frequency	For F _{in} = 2100 MHz	I _{CC_DYN} ^(1,4)		25	33	mA
Additive Output Supply Current per LVPECL Bank enabled		I _{CCO_PECL}		137	164	mA
Additive Output Supply Current per LVDS Bank enabled		I _{CCO_LVDS}		40	49	mA

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Output Supply Current per HCSL Bank enabled		I_{CCO_HCSL}		93	112	mA
Additive Output Supply Current, LVCMOS Output Enabled	$F_{IN} = 200 \text{ MHz}, C_{LOAD} = 5 \text{ pF}, V_{CCO} = 3.3 \text{ V}$	I_{CCO_CMOS}		6	7.2	mA
	$F_{IN} = 200 \text{ MHz}, C_{LOAD} = 5 \text{ pF}, V_{CCO} = 2.5 \text{ V}$			4.5	5.5	mA
Power Supply Rejection Ratio						
Ripple Induced Phase Spur Level, Supply Ripple of 100 mV pp	$F_{IN} = 156.25 \text{ MHz}, \text{Foffset} = 100 \text{ KHz}, V_{CCO/A/B} = 2.5 \text{ V}$	$PSRR_{PECL}$		-67		dBc
Ripple Induced Phase Spur Level, Supply Ripple of 100 mV pp	$F_{IN} = 156.25 \text{ MHz}, \text{Foffset} = 100 \text{ KHz}, V_{CCO/A/B} = 2.5 \text{ V}$	$PSRR_{LVDS}$		-70		dBc
Ripple Induced Phase Spur Level, Supply Ripple of 100 mV pp	$F_{IN} = 156.25 \text{ MHz}, \text{Foffset} = 100 \text{ KHz}, V_{CCO/A/B} = 2.5 \text{ V}$	$PSRR_{HCSL}$		-67.7		dBc
Input High Current	$V_{CC} = 3.3 \text{ V}, V_{IH} = V_{CC}$	I_{IH}		30	50	μA
Input Control Pin Characteristic						
Input Low Current		I_{IL}	-20	0.1		μA
Input High Voltage – Logic Inputs		V_{IH}	$0.7 \cdot V_{CC}$		V_{CC}	V
Input Low Voltage – Logic Inputs		V_{IL}	GND		$0.3 \cdot V_{CC}$	V
Internal Pull-down Resistance		$R_{pull\downarrow}$		200		K Ω

Notes:

1. Total current from core supply at frequency $F_{IN} = I_{CORE_STATIC} + N \cdot (0.5 \cdot F_{IN} / 2100 \text{ M}) \cdot I_{CORE_DYN}$. Detailed methodology of calculating the power dissipated in each ODR mode is given in the section "Current consumption and Power Dissipation Calculations." N is the number of output banks enabled.
2. Refer to [Application Information](#) section for more information on current consumption and power dissipation calculations.
3. Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: $DJ (\text{ps pk-pk}) = [(2 \cdot 10^{(PSRR / 20)}) / (\pi \cdot f_{CLK})] \cdot 1 \text{E}^{12}$
4. Specification is ensured by characterization and is not tested in production.

Table 4. Input Clock Characteristics

Unless otherwise specified: $V_{CC} = 3.3 \text{ V} \pm 5\%$, $2.5 \text{ V} \pm 5\%$, $V_{CCO} = 3.3 \text{ V} \pm 5\%$, $2.5 \text{ V} \pm 5\%$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $CLK_{IN0/1}$ driven differentially, input slew rate $\geq 3 \text{ V/ns}$. Typical values represent most likely parametric norms at $V_{CC} = 3.3 \text{ V}$, $V_{CCO} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Characteristics of Universal Input Clock Pins						
Input frequency range ^[4]		$F_{CLKIN}^{[1]}$	DC		2100	MHz
Differential input high voltage	CLKin driven differentially	V_{IHD}			V_{CC}	V
Differential input low voltage		V_{ILD}	GND			V
Peak differential input voltage swing ^[2]		V_{ID}	0.15		1.3	V
Differential input common mode voltage	Input differential swing of 150 mV	V_{CMD}	0.25		$V_{CC}-1.2$	V
	Input differential swing of 350 mV		0.25		$V_{CC}-1.1$	V
	Input differential swing of 800 mV		0.25		$V_{CC}-0.9$	V
Single ended input high voltage	Inverting differential input held at $V_{CC}/2$, $V_{CC} = 3.3 \text{ V}$	V_{IH}	2		V_{CC}	V
	Inverting differential input held at $V_{CC}/2$, $V_{CC} = 2.5 \text{ V}$		1.6		V_{CC}	

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Single ended input low voltage	Inverting differential input held at $V_{CC}/2$, $V_{CC} = 3.3\text{ V}$	V_{IL}	GND		1.3	V
	Inverting differential input held at $V_{CC}/2$, $V_{CC} = 2.5\text{ V}$		GND		0.9	
Single ended input voltage swing ^[3]		V_{I_SE}	0.3		V_{CC}	V_{PP}
Single ended input common mode voltage		V_{CM}	0.25		$V_{CC}-1.2$	V
Mux Isolation between the two input clock paths	$F_{IN} = 100\text{ MHz}$, Foffset > 50 KHz	$ISO_{MUX}^{[1]}$		-84		dBc
	$F_{IN} = 200\text{ MHz}$, Foffset > 50 KHz			-82		dBc
	$F_{IN} = 500\text{ MHz}$, Foffset > 50 KHz			-71		dBc
	$F_{IN} = 1000\text{ MHz}$, Foffset > 50 KHz			-65		dBc
Crystal Characteristics						
Equivalent series resistance		ESR		35	60	Ω
Load capacitance		CL	6	8	10	pF
Shunt Capacitance		Co		2	3	pF
Power dissipated in the crystal		Drive level		100	200	μW
Mode of oscillation			Fundamental			
Crystal frequency range		$F_{OSC}^{[1]}$	8		50	MHz
External clock frequency range	XO over drive or Bypass mode	F_{CLK}			250	MHz
Maximum swing level on OSC _{IN} /OSC _{OUT} pins	XO over drive or Bypass mode	V_{max}			1.8	V_{pp_se}
V_{ih_se}	Bypass DC coupled mode. SEL[1] = 1 & SEL[0]=1	V_{ih}	0.98			V
V_{il_se}		V_{il}			0.36	V
Crystal Phase jitter ^[4]	RMS, integration BW 12 KHz to 5 MHz, $F_{crystal} = 25\text{ MHz}$. Crystal input select Measured at $V_{CC} = V_{CCO} = 2.5\text{ V}$	$t_{jit}^{[1]}$		155		fs

Notes:

1. Specification is ensured by characterization and is not tested in production.
2. Refer to [Parameter Measurement Information](#) section for definition of VID and VOD voltages.
3. If the input clock is initially absent when the chip is just powered up, it will take atleast 2 falling edge of clock cycles for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edge of input clock
4. Crystal Phase Jitter is measure on following part number, 7M-25.000MAKV-T.

Table 5. Output Clock Characteristics – LVPECL

Unless otherwise specified: $V_{CC} = 3.3\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, $V_{CCO} = 3.3\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $\text{CLK}_{IN0/1}$ driven differentially, input slew rate $\geq 3\text{ V/ns}$. Typical values represent most likely parametric norms at $V_{CC} = 3.3\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$. Termination is $50\ \Omega$ to $V_{CCO} - 2\text{ V}$.

Parameters	Condition	Symbol	Min	Typ	Max	Unit
Maximum output frequency, full VOD swing $\geq 600\text{ mV}$ ^[1]	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	$F_{\text{CLKOUT_F}}$ ^[1]	1000	1200	-	MHz
Maximum output frequency, full VOD swing $\geq 400\text{ mV}$ ^[1]			1500	2100		MHz
Additive RMS jitter ^[1]	Integration bandwidth from 10 KHz to 20 MHz, $F_{\text{IN}} = 156.25\text{ MHz}$, $\text{SR} > 3\text{ V/ns}$ 50 Ω termination biased with $V_{CCO} - 2\text{ V}$	Jitter _{ADD} ^[1]		55	88	fs(rms)
Noise floor for Foffset > 10 MHz	50 Ω termination biased with $V_{CCO} - 2\text{ V}$, $F_{\text{IN}} = 156.25\text{ MHz}$, $\text{SR} > 3\text{ V/ns}$	Noise _{FLOOR} ^[1]		-159		dBc
Output Duty Cycle	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	ODC	45		55	%
Output High Voltage	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	V_{OH}	$V_{CCO} - 1.165$		$V_{CCO} - 0.75$	V
Differential Output Voltage	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	V_{OD}	475	678	960	mV
Output Low Voltage	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	V_{OL}	$V_{CCO} - 2.0$		$V_{CCO} - 1.45$	V
Output Rise Time, 20% to 80%	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	t_{R}		210		ps
Output Fall Time 20% to 80%	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	t_{F}		210		ps
Input to Output Delay	50 Ω termination biased with $V_{CCO} - 2\text{ V}$	t_{pd}		700	900	ps
Skew between Outputs from same Bank (Absolute Max)	$V_{CCO} = 3.3\text{ V}$, 2.5 V	T_{sk}			60	ps

Notes:

1. Specification is guaranteed by characterization and is not tested in production.

Table 6. Output Clock Characteristics - LVDS

Unless otherwise specified: $V_{CC} = 3.3\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, $V_{CCO} = 3.3\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $\text{CLK}_{IN0/1}$ driven differentially, input slew rate $\geq 3\text{ V/ns}$. Typical values represent most likely parametric norms at $V_{CC} = 3.3\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Maximum Output Frequency, Full VOD Swing $\geq 250\text{ mV}$	$R_L = 100\ \Omega$, differential	$F_{\text{CLKOUT_FS}}$ ^[1]	1000	1600	-	MHz
Maximum Output Frequency, Full VOD Swing $\geq 200\text{ mV}$	$R_L = 100\ \Omega$, differential		1500	2100		MHz
Additive RMS Jitter	Integration bandwidth from 10 KHz to 20 MHz, $F_{\text{IN}} = 156.25\text{ MHz}$, $\text{SR} > 3\text{ V/ns}$ $R_L = 100\ \Omega$, differential	Jitter _{ADD}		60	82	fs(rms)
Noise Floor for Foffset > 10 MHz	$F_{\text{IN}} = 156.25\text{ MHz}$, $\text{SR} > 3\text{ V/ns}$ $R_L = 100\ \Omega$, differential	Noise _{FLOOR}		-159		dBc
Output Duty Cycle	$R_L = 100\ \Omega$, differential	ODC	45		55	%
Change in VPP between Complementary Output States	$R_L = 100\ \Omega$, differential	ΔVPP			50	mV
Output Differential Peak Voltage	$R_L = 100\ \Omega$, differential, 156.25M	V_{OD}	300		420	mV

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Common-Mode Voltage	$R_L = 100\ \Omega$, differential	V_{OCM}	1.125	1.2	1.375	V
Output Rise Time, 20% to 80%	$R_L = 100\ \Omega$, differential, $C_L < 5\ \text{pF}$	t_R		210		ps
Output Fall Time 20% to 80%	Uniform transmission line up to 10 inches with characteristic impedance of $50\ \Omega$	t_F		210		ps
Input to Output Delay		t_{pd}		700	900	ps
Skew between Outputs from same Bank (Absolute Max)	$V_{CCO} = 3.3\ \text{V}, 2.5\ \text{V}$	T_{sk}			60	ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 7. Output Clock Characteristics – HCSL

Unless otherwise specified: $V_{CC} = 3.3\ \text{V} \pm 5\%$, $2.5\ \text{V} \pm 5\%$, $V_{CCO} = 3.3\ \text{V} \pm 5\%$, $2.5\ \text{V} \pm 5\%$, $1.8\ \text{V} \pm 5\%$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, CLKIn0/1 driven differentially, input slew rate $\geq 3\ \text{V/ns}$. Typical values represent most likely parametric norms at $V_{CC} = 3.3\ \text{V}$, $V_{CCO} = 3.3\ \text{V}$, $T_A = 25^\circ\text{C}$.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Maximum Output Frequency	$R_L = 50\ \Omega$ to GND	$F_{CLKOUT_F}^{[1]}$	DC		700	MHz
Additive RMS Jitter	Integration bandwidth from 10 KHz to 20 MHz, $F_{IN} = 156.25\ \text{MHz}$, $SR > 3\ \text{V/ns}$ $R_L = 50\ \Omega$ to GND	$Jitter_{ADD}^{[1]}$		55	86	fs(rms)
Noise Floor for Foffset > 10 MHz		$Noise_{FLOOR}^{[1]}$		-159		dBc
Output Duty Cycle		ODC	45		55	%
Output Low Voltage Min	$R_L = 50\ \Omega$ to GND at far end; $50\ \Omega$ controlled impedance transmission line Supply voltage: $1.8\ \text{V} \pm 5\%$, $2.5\ \text{V} (\pm 10\%)$, $3.3\ \text{V} (\pm 10\%)$	$V_{MIN}(\text{transient})$	-200			mV
Single-Ended Output High Voltage	$R_L = 50\ \Omega$ to GND	V_{OH}	600	840	1150	mV
Single-Ended Output Low Voltage		V_{OL}	-150	28	150	mV
Absolute Crossing Point Voltage	$R_L = 50\ \Omega$ to GND, $C_L < 5\ \text{pF}$	V_{CROSS}	250		550	mV
Variation of V_{CROSS} over all Rising Clock Edges		$V_{CROSS\ DELTA}$			140	mV
Skew between P and N Rails	$R_L = 50\ \Omega$ to GND at far end; $50\ \Omega$ controlled impedance transmission line; PCB routing skew $< 1\ \text{ps}$ Supply voltage: $2.5\ \text{V} (\pm 10\%)$, $3.3\ \text{V} (\pm 10\%)$	P-NSKEW	< abs (50)			ps
Output Rise Time, 20% to 80%	$F_{IN} = 156.25\ \text{MHz}$, Uniform transmission line up to 10 inches with characteristic impedance of $50\ \Omega$ $R_L = 50\ \Omega$ to GND, $C_L < 5\ \text{pF}$	t_R		210		ps
Output Fall Time, 20% to 80%		t_F		210		ps
Input to Output Delay		t_{pd}		825	1100	ps
Skew between outputs from same bank (Absolute max)	$V_{CCO} = 3.3\ \text{V}, 2.5\ \text{V}$	T_{sk}			60	ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 8. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architecture

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	PCIe Gen 1 ^[1,2,3,4]	$t_{jphPCIeG1-CC}$		2	5	ps (p-p)
	PCIe Gen 2 ^[1,2,3,4]	$t_{jphPCIeG2-CC}$		0.08	0.15	ps(rms)
	PCIe Gen 3 ^[1,2,4,6]	$t_{jphPCIeG3-CC}$		0.03	0.07	
	PCIe Gen4 ^[1,2,4,6]	$t_{jphPCIeG4-CC}$		0.03	0.07	
	PCIe Gen5 ^[1,2,4,6]	$t_{jphPCIeG5-CC}$		0.01	0.022	
	PCIe Gen6 ^[1,2,4,6]	$t_{jphPCIeG6-CC}$		0.008	0.014	
	PCIe Gen7 ^[1,2,4,6]	$t_{jphPCIeG7-CC}$		0.006	0.01	

Notes:

1. Applies to all the differential outputs, guaranteed by design and characterization.
2. Applies to all the Outputs when driven by a low phase noise source SMA100B.
3. Additive RMS Jitter Measurements were made using DSA90804A for minimum waveform length of $\geq 100k$ cycles with a minimum sampling rate of $\geq 40GSa/s$ with the waveform covering 90% of the DSO screen. All the post processing the DSO is disabled to decrease the additional jitter impact from oscilloscope. Broadband oscilloscope noise is also minimized in the measurement.
4. Additive jitter for RMS values is calculated by solving the equation for b [$b = \sqrt{c^2 - a^2}$] where 'a' the rms input jitter and "c" is the rms total jitter.
5. Input to SiT92208 is fed using low phase noise source SMA100B, SiT92208 is configured as 100MHz HCSL Output Driver [$V_{CCOX} = 3.3V$] and fed to the channels of DSA90804A using the exact measurement set up [Refer Note 6].
6. SiT92208 PCI Express Additive RMS Jitter Measurement Set up configuration.

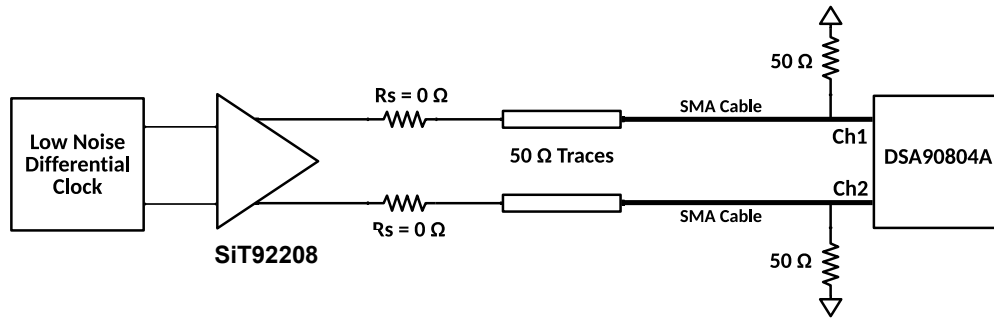


Table 9. Output Clock Characteristics – LVCMOS

Unless otherwise specified: $V_{CC} = 3.3 V \pm 5\%$, $V_{CCO} = 3.3 V \pm 5\%$, $2.5 V \pm 5\%$, $1.8 V \pm 5\%$, $-40^\circ C \leq T_A \leq 85^\circ C$, $CLK_{IN0/1}$ driven differentially, input slew rate $\geq 3 V/ns$. Typical values represent most likely parametric norms at $V_{CC} = 3.3 V$, $V_{CCO} = 3.3 V$, $T_A = 25^\circ C$.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Frequency		f_{CLKOUT}	0		250	MHz
Additive RMS Jitter Freq = 156.25M ; Integration Bandwidth 12 kHz to 20 MHz	$V_{CCO} = 3.3 V \pm 5\%$	$Jitter_{ADD}^{(1)}$		30	50	fs rms
	$V_{CCO} = 2.5 V \pm 5\%$			40	60	
	$V_{CCO} = 1.8 V \pm 5\%$			90	150	
Output Duty Cycle	For $F_{in} \leq 200$ MHz	ODC	45		55	%
	For $200 \text{ MHz} < F_{in} < 250$ MHz		40		60	%
Output high voltage	$V_{CCO} = 3.3 V \pm 5\%$, 1 mA pull down current	V_{OH}	$V_{CCO} - 0.1 V$			V
	$V_{CCO} = 2.5 V \pm 5\%$, 1 mA pull down current		$V_{CCO} - 0.1 V$			V
Output low voltage	$V_{CCO} = 3.3 V \pm 5\%$, 1 mA pull up current	V_{OL}			0.1	V
	$V_{CCO} = 2.5 V \pm 5\%$, 1 mA pull up current				0.1	V
Output rise time, 20% to 80%	$C_{LOAD} = 5 \text{ pF}$, $R_{LOAD} = 50 \Omega$ AC coupled	t_r		250	450	ps
Output fall time 20% to 80%		t_f		250	450	ps
Output enable time		$t_{EN}^{(1)}$			4	cycles
Output disable time		$t_{DIS}^{(1)}$			4	cycles
Input to clock edge to output clock edge delay	$V_{CCO} = 3.3 V$, PCB trace of 5 inch, 5 pF capacitor	$t_d^{(1)}$		1.4	2.5	ns
	$V_{CCO} = 2.5 V$, PCB trace of 5 inch, 5 pF capacitor			1.5	2.7	ns

Notes:

1. Specification is ensured by characterization and is not tested in production.

Pin Configuration

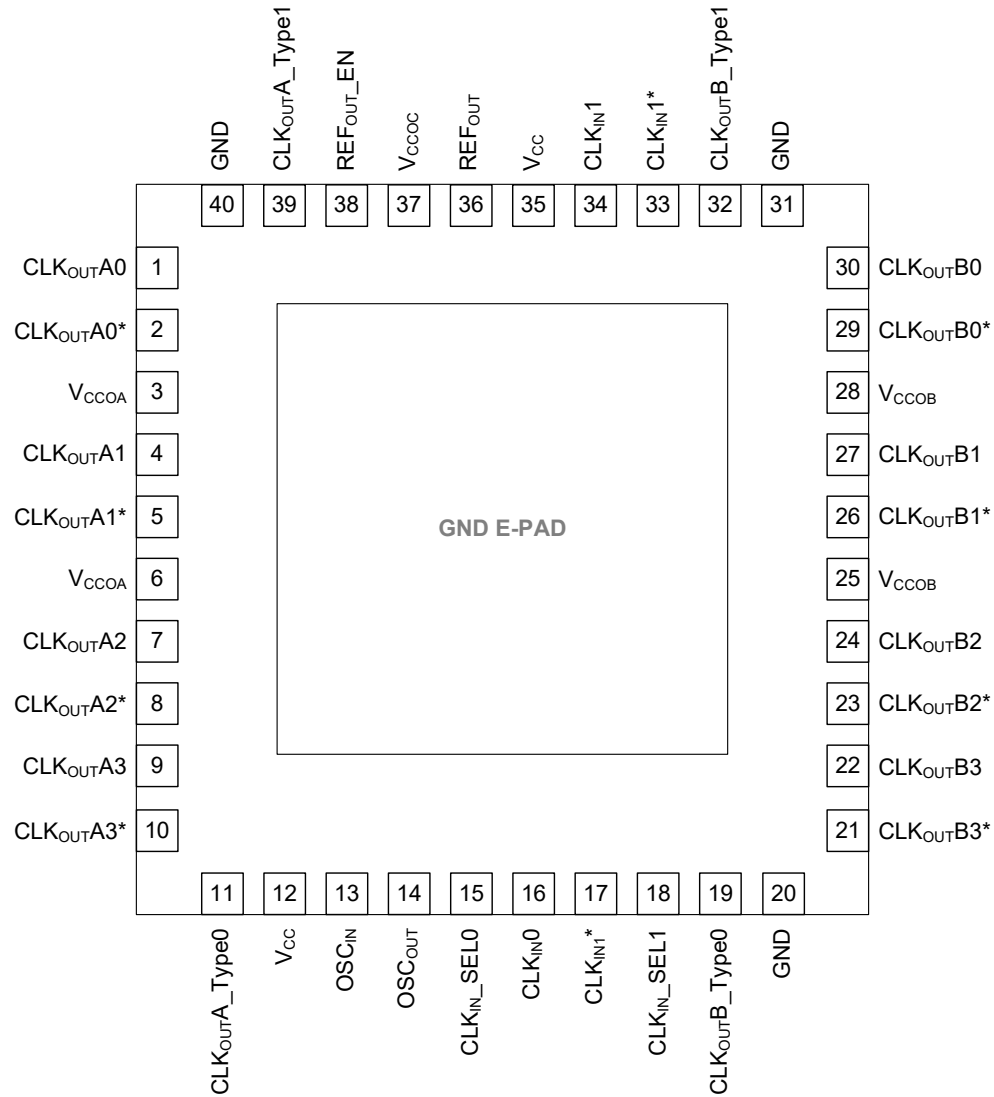


Figure 2. SiT92208 Pin Configuration Top View

Table 10. Pin Description

Pin Name	Pin Number	Functionality SiT92208
Pin group: Bank A clock output pads		
CLK_OUTA0	1	Differential clock output P of A0. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA0*	2	Differential clock output N of A0. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA1	4	Differential clock output P of A1. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA1*	5	Differential clock output N of A1. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA2	7	Differential clock output P of A2. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA2*	8	Differential clock output N of A2. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA3	9	Differential clock output P of A3. Output type set by CLK_OUTA_TYPE pins.
CLK_OUTA3*	10	Differential clock output N of A3. Output type set by CLK_OUTA_TYPE pins.
Pin group: Bank B clock output pads		
CLK_OUTB0	30	Differential clock output P of B0. Output type set by CLK_OUTB_TYPE pins.

Pin Name	Pin Number	Functionality SiT92208
CLK _{OUT} B0*	29	Differential clock output N of B0. Output type set by CLK _{OUT} B_TYPE pins.
CLK _{OUT} B1	27	Differential clock output P of B1. Output type set by CLK _{OUT} B_TYPE pins.
CLK _{OUT} B1*	26	Differential clock output N of B1. Output type set by CLK _{OUT} B_TYPE pins.
CLK _{OUT} B2	24	Differential clock output P of B2. Output type set by CLK _{OUT} B_TYPE pins.
CLK _{OUT} B2*	23	Differential clock output N of B2. Output type set by CLK _{OUT} B_TYPE pins.
CLK _{OUT} B3	22	Differential clock output P of B3. Output type set by CLK _{OUT} B_TYPE pins.
CLK _{OUT} B3*	21	Differential clock output N of B3. Output type set by CLK _{OUT} B_TYPE pins.
Pin group: Bank C clock output pad		
REF _{OUT}	36	LVC MOS clock out synchronized with differential clocks
Pin group: Clock inputs		
CLK _{IN} 0	16	Universal clock input 0 (+ve polarity) (differential/single-ended)
CLK _{IN} 0*	17	Universal clock input 0 (-ve polarity) (differential/single-ended)
CLK _{IN} 1	34	Universal clock input 1 (+ve polarity) (differential/single-ended)
CLK _{IN} 1*	33	Universal clock input 1 (-ve polarity) (differential/single-ended)
OSC _{IN}	13	Input for crystal. It can be over driven by an AC coupled single ended clock in crystal over drive mode.
		In the external bypass mode, the max voltage at the pin needs to be 1.5 V. If the driver is swinging to say 3.3 V rail, then a resistor divider is needed on PCB to restrict the swing at OSC _{IN} to 1.5V
		Load supported 6pF to 10pF, freq 8 MHz to 50 MHz
OSC _{OUT}	14	Output for crystal. Leave OSC _{OUT} floating if OSC _{IN} is driven by a single-ended clock.
Pin group: Power pins		
V _{CC}	12	Line supply - 3.3 V/2.5 V
V _{CC}	35	Line supply - 3.3 V/2.5 V
V _{CCOA}	3	Power supply for Bank A Output buffers. V _{CCOA} can operate from 3.3 V or 2.5 V
V _{CCOA}	6	Power supply for Bank A Output buffers. V _{CCOA} can operate from 3.3 V or 2.5 V
V _{CCOB}	25	Power supply for Bank A Output buffers. V _{CCOA} can operate from 3.3 V or 2.5 V
V _{CCOB}	28	Power supply for Bank A Output buffers. V _{CCOA} can operate from 3.3 V or 2.5 V
V _{CCOC}	37	Power supply for Bank C Output buffer. V _{CCOC} can operate from 3.3 V or 2.5 V or 1.8 V
GND-EPAD	0	Ground
GND	20	Ground pin
GND	31	Ground pin
GND	40	Ground pin
Pin group: Control pins		
CLK _{OUT} A_Type0	11	Bank A output buffer type selection pins
CLK _{OUT} A_Type1	39	Bank A output buffer type selection pins
CLK _{OUT} B_Type0	19	Bank B output buffer type selection pins
CLK _{OUT} B_Type1	32	Bank B output buffer type selection pins
REF _{OUT} _EN	38	REF _{OUT} enable input. Enable signal is internally synchronized to selected clock input.
CLK _{IN} _SEL0	15	Clock input selection pins
CLK _{IN} _SEL1	18	Clock input selection pins

Functional Description

The SiT92208 is a 8-output differential clock fan out buffer with low additive jitter that can operate up to 2.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 4 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVC MOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 40-pin WQFN package.

V_{CC} and V_{CCO} Power Supplies

The SiT92208 has separate 3.3/2.5 core (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}). HCSL can support 1.8V power supplies (V_{CCOA}, V_{CCOB}). V_{CCOC} supply can operate on 3.3 V/2.5 V/1.8 V rail. Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVC MOS (V_{OH}) are referenced to its respective V_{CCO} supply, while the output levels for LVDS and HCSL are relatively constant over the specified V_{CCO} range.

Clock Inputs

The input clock can be selected from CLK_{IN0}/CLK_{IN0}*, CLK_{IN1}/CLK_{IN1}*, or OSC_{IN}. Clock input selection is controlled using the CLK_{IN_SEL}[1:0] inputs as shown in Table 11. When CLK_{IN0} or CLK_{IN1} are selected, the oscillator is power down. The user can float OSC_{IN} and OSC_{OUT} pins, since these pins are internally pulled down. OSC_{IN} is pulled down with a 56 kΩ resistance.

Table 11. Input Clock Selection

CLK _{IN_SEL} [1]	CLK _{IN_SEL} [0]	Selected Clock
0	0	CLK _{IN0} , CLK _{IN0} *
0	1	CLK _{IN1} , CLK _{IN1} *
1	0	Crystal Or Crystal Bypass AC Coupled mode
1	1	Crystal Bypass DC Coupled mode

Clock States (Input vs Output States)

Table 12. Input versus Output Stages

State of Selected Clock input	Output State
Inputs are floating	Logic low
Inputs are logic low	Logic low
Inputs are logic high	Logic high

Output Driver Type

The differential output buffer type for Bank A and Bank B outputs can be separately configured using the CLK_{OUTA_TYPE}[1:0] and CLK_{OUTB_TYPE}[1:0] inputs, respectively, as shown Table 13. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, it is recommended to disable (Hi-Z) the bank to reduce power.

Table 13. OE Functionality

CLK _{OUTX_TYPE} 1	CLK _{OUTX_TYPE} 0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

Reference Output

The reference output (REF_{OUT}) provides a LVC MOS copy of the selected input clock. The LVC MOS output high level is referenced to the V_{CCOC} voltage. REF_{OUT} can be enabled or disabled using the enable input pin, REF_{OUT_EN}, as shown in Table 14. The reference output clock is internally synchronized to the selected clock. This avoids any glitches or runt pulses while enabling or disabling the reference clock. Pulling REF_{OUT_EN} to LOW, forces the outputs to the high-impedance state with in 4 falling edges of the input signal. The outputs remain in the high-impedance state as long as REF_{OUT_EN} is LOW. When REF_{OUT_EN} goes from HIGH to LOW, the output clock is disabled within 4 falling edges of the input clock signal. The output is disabled at the falling edge of the input clock. This allows to disable the output clock in a glitch free manner.

When REF_{OUT_EN} goes from low to high, the output clock is enabled within a time delay t_d, where t_d is given by the following equation.

$$t_{d,refout_en} = 0.5n + 3 * T_{in}.$$

Where, T_{in} is the time period of the input clock.

When REF_{OUT_EN} is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REF_{OUT_EN} is configured with a 1K Ω load to ground, then the output will be pulled to low when disabled.

Table 14. Reference Output Enable

Ref _{OUT_EN}	Output State
0	Disabled (HiZ)
1	Enabled

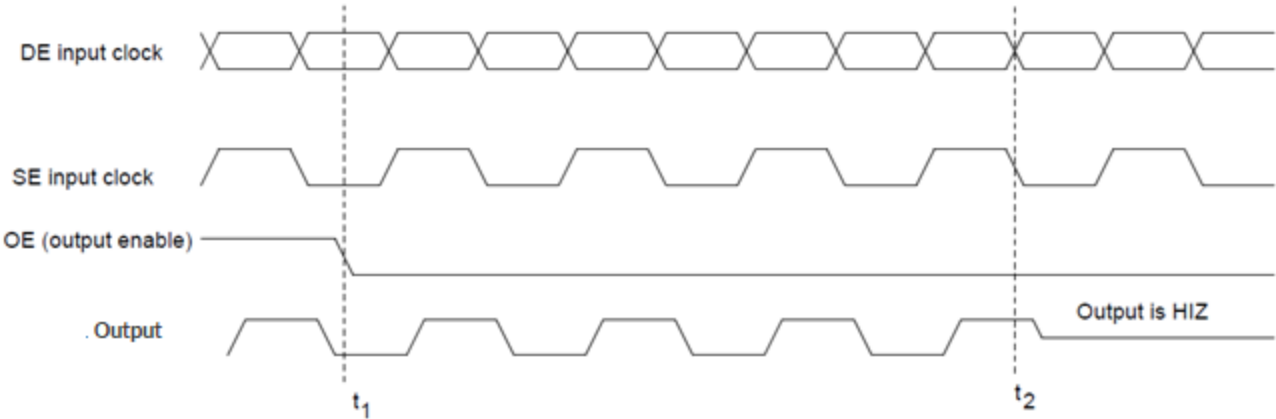


Figure 3. REF_{OUT_EN}: Output disable

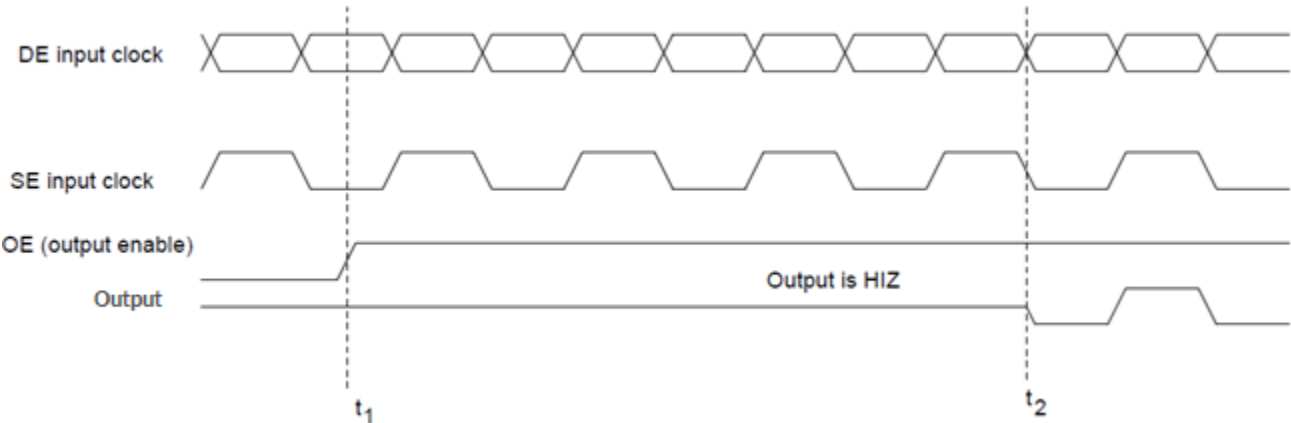


Figure 4. REF_{OUT_EN}: Output enable

Application Information

Current consumption and Power Dissipation Calculations

The current consumption specified in the Electrical Characteristics can be used to calculate the total power dissipation and the IC power dissipation for any output driver configuration. The total current drawn from the V_{CC} is given by the equation below.

$$I_{CC} = I_{CORE,STATIC} + n * \left(\frac{f_{in}}{100} \right) * I_{CORE,DYN}$$

- I_{CC} , is the total core current drawn from V_{CC} .
- $I_{CORE,STATIC}$, is the current drawn by SiT92208, when clocks are not toggling and both the output driver banks are in HIZ state.
- $I_{CORE,DYN}$, is the switching current taken from V_{CC} when the selected input clock is toggling at a frequency of f_{in} .
- n , is the number of output banks that are active.

Current consumed by the output supplies in each mode are listed below.

- The current in output bank A/B in LVPECL mode is
 $I_{CCOA} = I_{CCOB} = I_{CC,LVPECL}$
- The current in output bank A/B in LVDS mode is
 $I_{CCOA} = I_{CCOB} = I_{CC,LVDS}$
- The current in output bank A/B in HCSL mode is
 $I_{CCOA} = I_{CCOB} = I_{CC,HCSL}$
- The current in output bank C is $I_{CCOC} = I_{CC,LVCMOS}$

The equation for the total power dissipation is

$$P_{TOTAL} = V_{CC} * I_{VCC} + V_{CCOA} * I_{CCOA} + V_{CCOB} * I_{CCOB} + V_{CCOC} * I_{CCOC}$$

If the output driver configuration is LVPECL or LVDS, then the power dissipated in any termination resistors and termination voltages need to be accounted to calculate the power dissipation in the device.

The power dissipated in the termination resistor in LVPECL mode is given below.

$$P_{RT_PECL} = \frac{(V_{OH_PECL} - V_{TT})^2}{R_T} + \frac{(V_{OL_PECL} - V_{TT})^2}{R_T}$$

The power dissipated in the termination voltage for LVPECL mode is given below

$$P_{VTT_PECL} = V_{TT} * \left(\frac{(V_{OH_PECL} - V_{TT})}{R_T} + \frac{(V_{OL_PECL} - V_{TT})}{R_T} \right)$$

The power dissipated in the ground referenced termination resistor for HCSL is given below

$$P_{RT_HCSL} = \frac{V_{OH_HCSL}^2}{R_T}$$

The power dissipated in the device is given below.

$$P_{DEVICE} = P_{TOTAL} - N_1 * (P_{RT_PECL} + P_{VTT_PECL}) - N_2 * P_{RT_HCSL}$$

Example: Worst case power dissipation

BANK A and BANK B output drivers are configured in HCSL mode. The input frequency is 2100 MHz. $V_{CC} = 3.465$ V, $V_{CCOA} = V_{CCOB} = V_{CCOC} = 3.465$ V, REF_{OUT} is disabled.

Table 15. Worst Case Power Dissipation

Parameter	Value	Unit
V_{CC}	3.465	V
V_{CCOA}	3.465	V
V_{CCOB}	3.465	V
V_{CCOC}	3.465	V
I_{CC}	49.2	mA
I_{CCOA}	115	mA
I_{CCOB}	115	mA
P_{TOTAL}	967	mW
V_{OH_HCSL}	0.83	V
V_{OL_HCSL}	0.044	V
P_{load}	159	mW
P_{DEVICE}	808	mW

Driving the Clock Inputs

The SiT92208 has two universal clock inputs (CLK_{IN0}/CLK_{IN0}^* and CLK_{IN1}/CLK_{IN1}^*). SiT92208 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The SiT92208 supports a wide common mode voltage range and input signal swing. To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter.

It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say CLK_{IN0} , then CLK_{IN0}^* pin need to be connected to a 0.1 uF capacitor on the PCB.

Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 5 shows how a differential input can be wired to accept LVCMOS single ended levels in AC coupled mode. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass should be located as close to the input pin as possible. Two resistors R_{T1} and R_{T2} set the common mode voltage at the output of the LVCMOS driver to $V_{CC}/2$. This prevents average DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{T1} and R_{T2} values should be adjusted to set the V1 at 1.25 V. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line

impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω .

$$Z_o = R_o + R_s = 50 \Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \Omega$$

$$\frac{V_{CC} * R_{T2}}{R_{T1} + R_{T2}} = \frac{V_{CC}}{2}$$

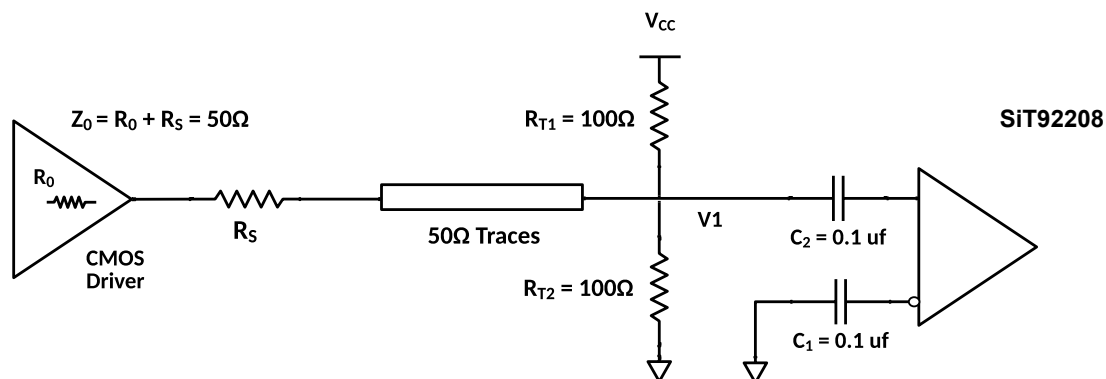


Figure 5. AC coupling LVCMOS clock to SiT92208

The inverting differential input can be connected to a 0.1 μ F bypass capacitor. This pin is biased internally to a voltage close to $V_{CC}/2$.

Another variant of the AC coupling of LVCMOS input clock is shown in Figure 6. We use single termination resistor of

50 Ω to ground. A 0.1 μ F (C_3) ac coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50 \Omega$$

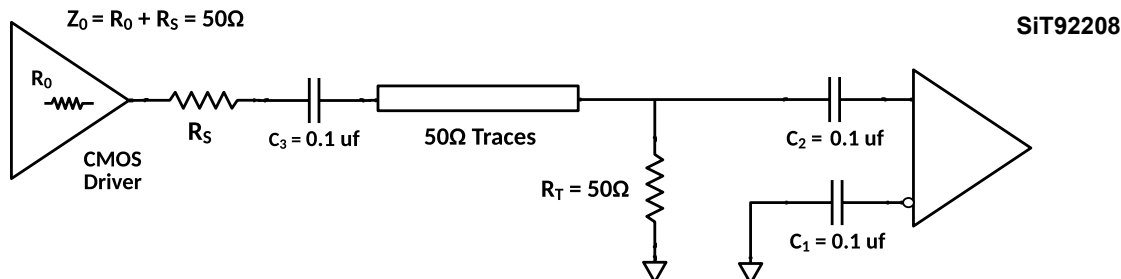


Figure 6. AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

Driving Clock Inputs with LVCMOS Driver (DC coupled)

Figure 7 shows how a differential input can be wired to accept LVCMOS single ended clock signals in DC coupled mode. The reference voltage $V1 = V_{CC}/2$ is generated by the bias resistors R_{S1} and R_{S2} . The bypass capacitor ($C1$) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage $V2$ in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50 \Omega$$

$$\frac{V_{CC} * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{CC}}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \Omega$$

$$\frac{V_{CC} * R_{T2}}{R_{T1} + R_{T2}} = \frac{V_{CC}}{2}$$

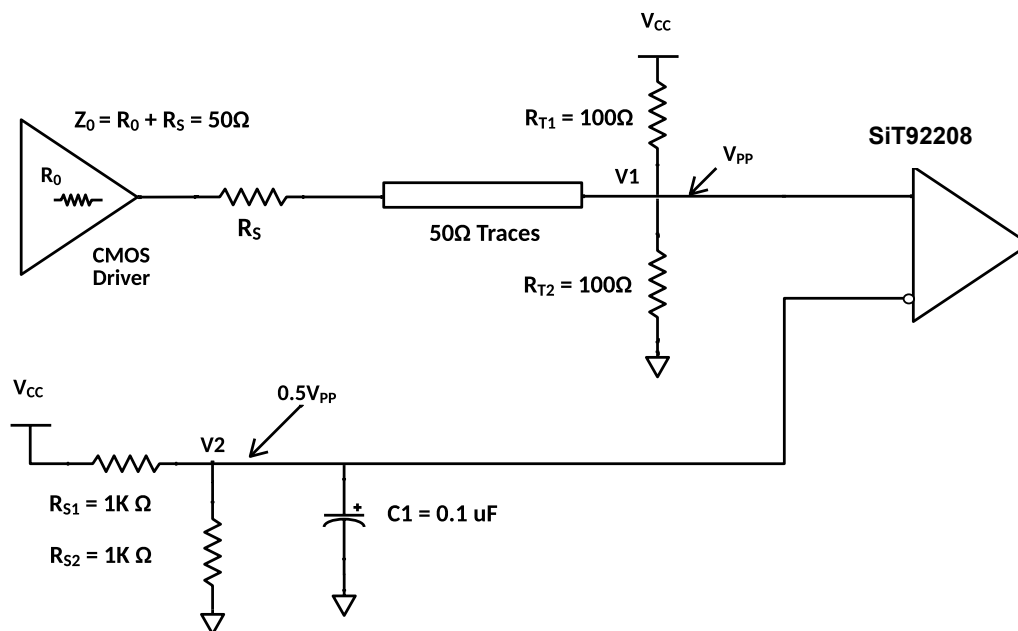


Figure 7. DC coupling of LVCMOS clock to SiT92208 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the $V2$ at 1.25 V. The values given below are for when both the single ended swing and V_{CC} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 8 shows a second input clock configuration where R_{T1} , R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50 Ω load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 8 is given below

$$Z_o = R_o + R_s = 50 \Omega$$

$$\frac{V_{CC} * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{pp}}{2}$$

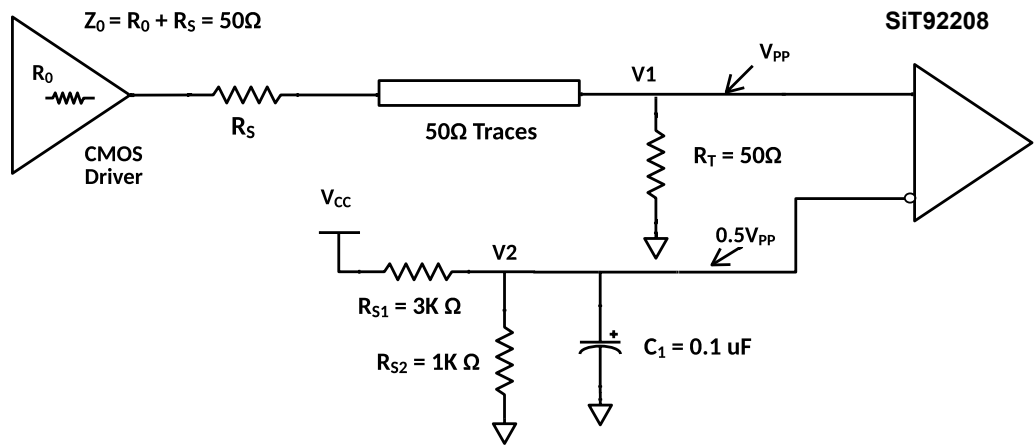


Figure 8. DC coupled LVCMOS input clock configuration – configuration 2

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 9. There is a single termination resistor R_T which is connected to ground through a capacitor C_{AC} .

The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega},$$

Where T_D is the transmission line delay

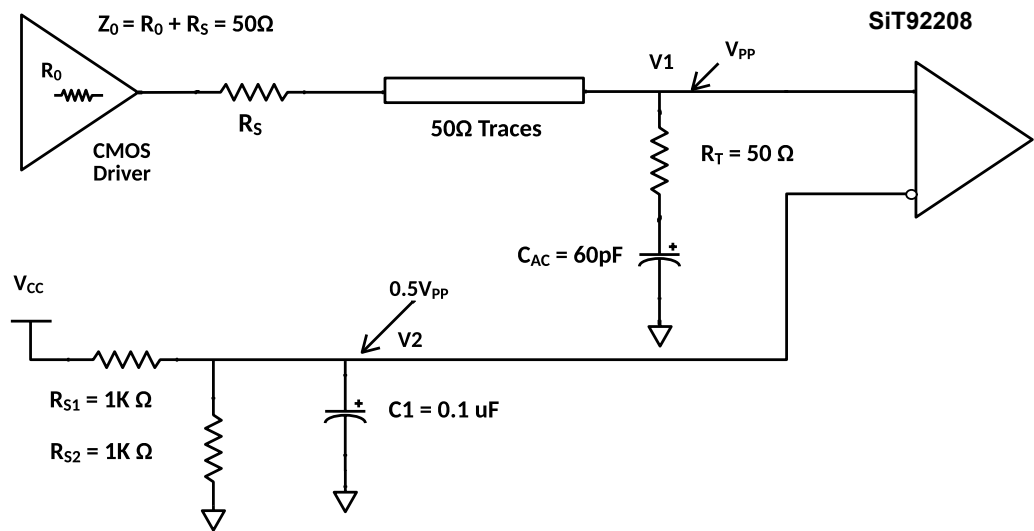


Figure 9. DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can direct couple the LVCMOS clock to SiT92208 input clock pin as shown in [Figure 10](#).

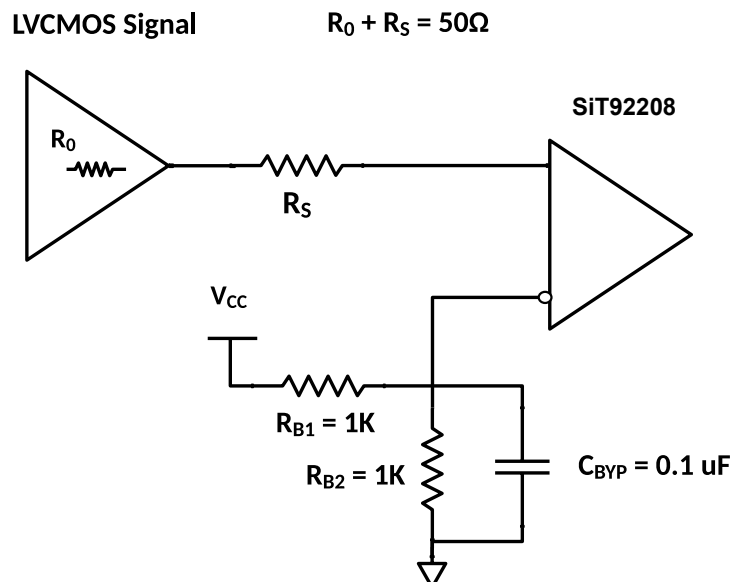


Figure 10. Direct coupling of LVCMOS clock to SiT92208

Driving OSC_{IN} with LVCMOS Driver (AC coupled)

The crystal input OSC_{IN} can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at OSC_{IN} should be limited to 1.8 V. The OSC_{OUT} pin, in this case can be floating. The SEL1, SEL0 should be 2'b10. The maximum voltage at OSC_{IN} should not exceed 1.8 V and minimum voltage should not go below -0.5 V. The slew rate at OSC_{IN} should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. [Figure 11](#) shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, RT1 and RT2 in parallel should

equal the transmission line impedance. For most 50 Ω applications, RT1 and RT2 can be 100 Ω.

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \text{ Ohm}$$

$$\frac{V_{cc} * R_{T2}}{R_{T1} + R_{T2}} = \frac{V_{cc}}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.8 V. The maximum DC bias voltage of OSC_{IN} is 0.675 V. Therefore the maximum swing at the OSC_{IN} pin is given by the equation given below.

$$V_{swing,pk,XTAL_IN} = 0.675 + 0.5 * 1.8 = 1.575V$$

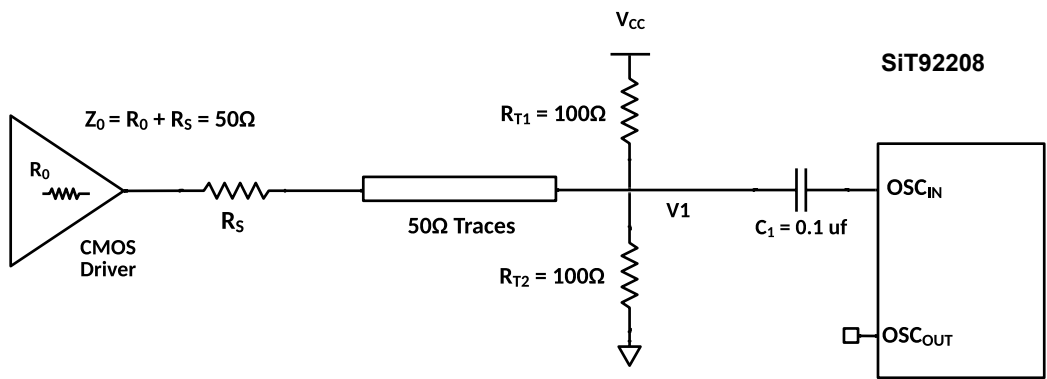


Figure 11. Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 12 shows a second input clock configuration where R_{T1} , R_{T2} are removed and replaced with a 50 Ω termination

resistor R_T to ground. A 0.1 uF is in series with the CMOS driver to prevent any DC leakage current.

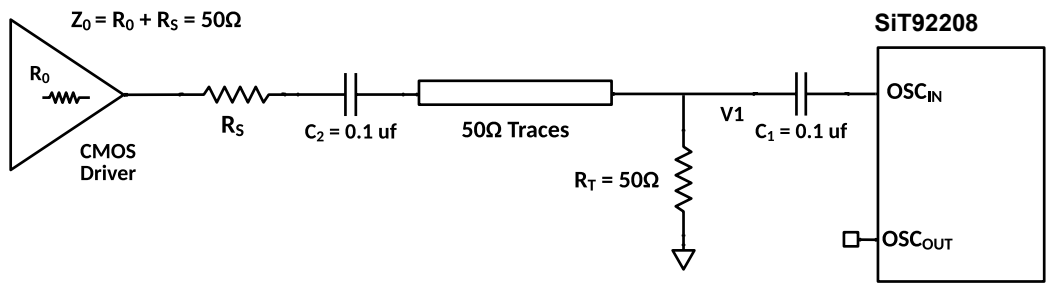


Figure 12. Single ended LVCMOS input – configuration 2, AC coupling to crystal input

Driving OSC_{IN} with LVCMOS Driver (DC coupled)

The crystal input OSC_{IN} can be overdriven with single ended clock as shown in Figure 13, in DC couple mode. The peak swing at OSC_{IN} should be limited to 1.8 V (voltage at the crystal input pin). The OSC_{OUT} pin, in this case can

be floating. The SEL1, SEL0 should be 2'b11. If the LVCMOS driver is on higher supply, say 3.3 V, use a resistor divider on the PCB to scale down the peak output voltage to 1.8 V.

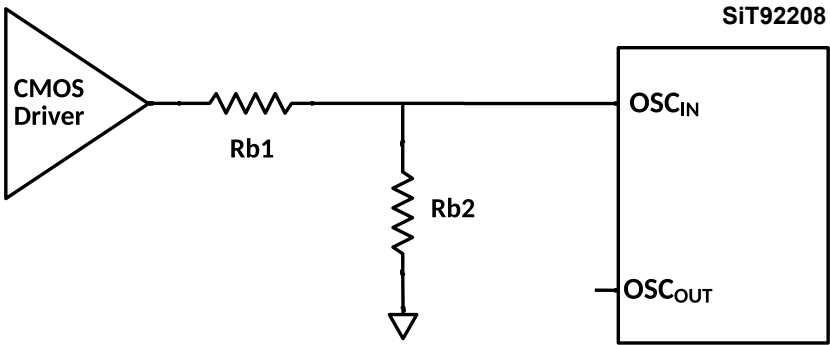


Figure 13. Single ended LVCMOS input, DC coupling to crystal input

LVDS (DC coupled)

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 14.

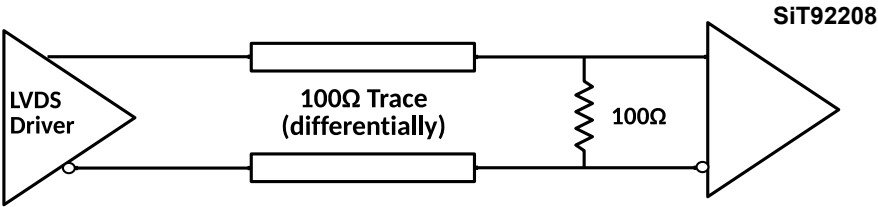


Figure 14. Termination scheme for DC coupled LVDS

HCSL (DC coupled)

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance R_s is sometimes used to limit the

overshoot during fast transients. The termination scheme is shown in Figure 15.

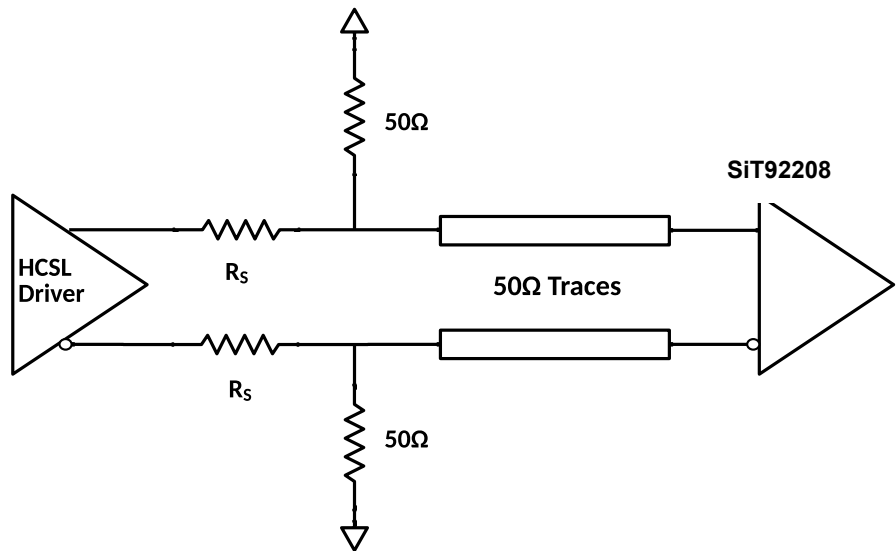


Figure 15. Termination scheme for DC coupled HCSL

LVPECL (DC coupled)

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source V_{TT} .

$$V_{TT} = V_{CCO} - 2V.$$

This termination scheme is shown in Figure 16. Alternatively, the user can also implement a Thevenin equivalent of V_{TT} using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 17.

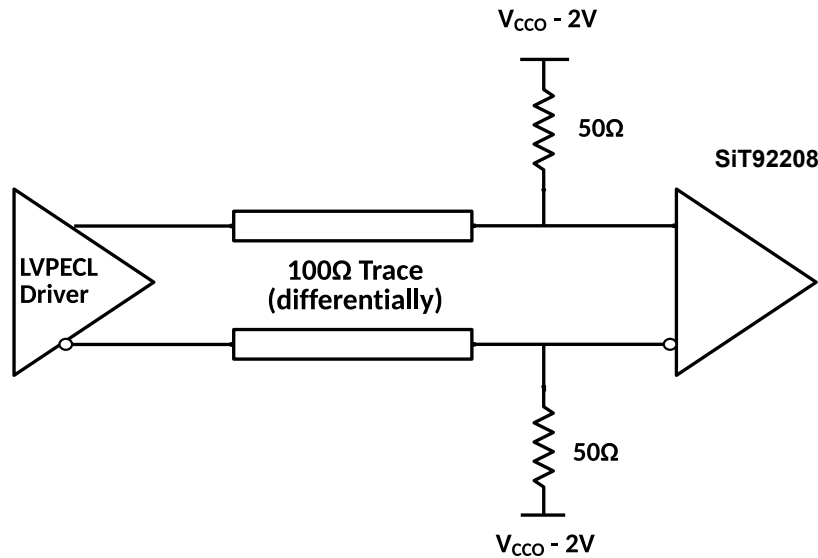


Figure 16. Termination scheme for DC coupled LVPECL

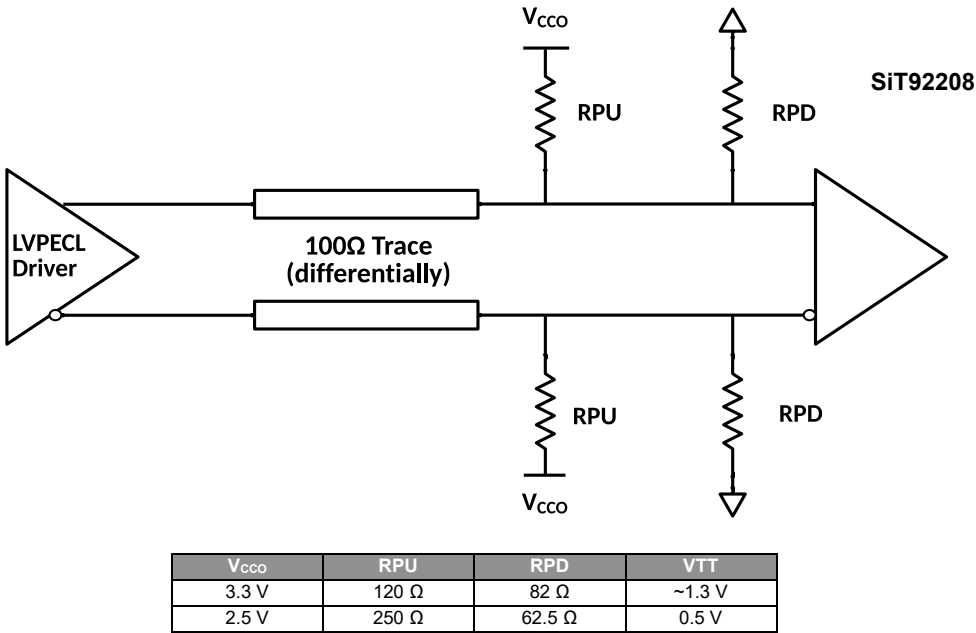


Figure 17. Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$
$$\frac{R_{PD} * V_{CCO}}{R_{PD} + R_{PU}} = V_{CCO} - 2V$$

SSTL (DC coupled)

The SSTL input clock configuration is shown in [Figure 18](#). The transmission line impedance is 60 Ω in the application example given. Therefore we use two 120 Ω resistors from V_{CCO} to ground for biasing the clock input pins. The effective termination impedance in this case is 60 Ω.

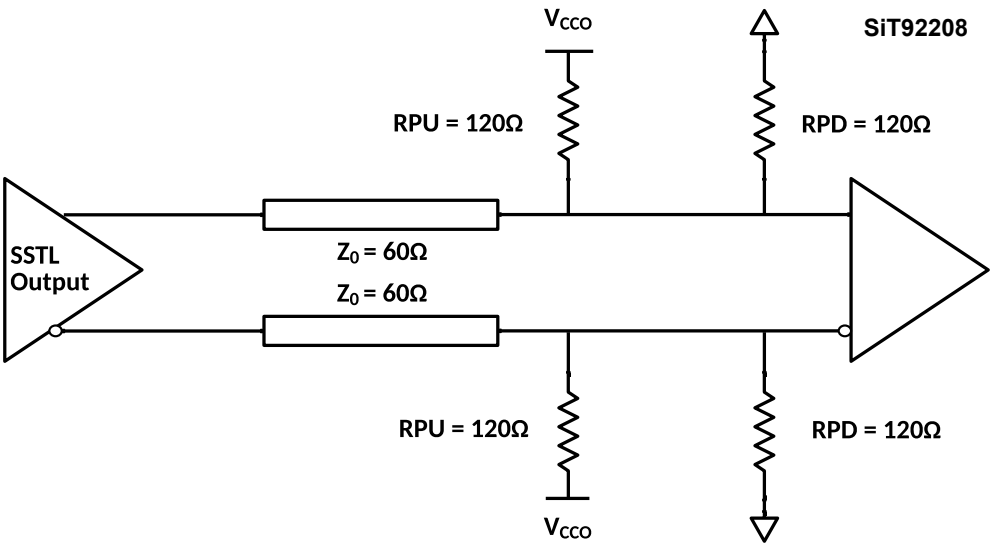


Figure 18. Example of input clock termination for SSTL clock.

LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in [Figure 19](#).

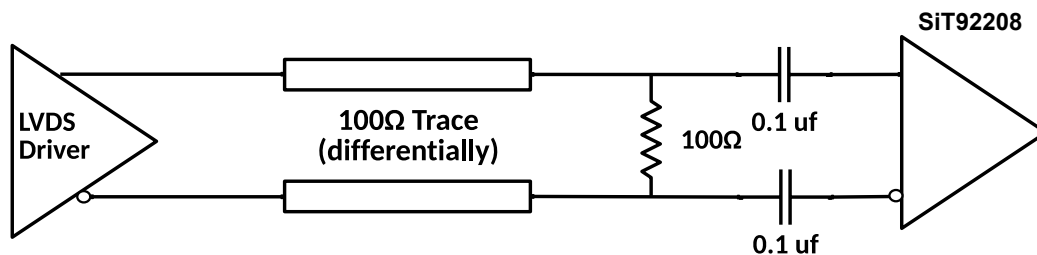


Figure 19. Termination scheme for AC coupled LVDS

The LVPECL should have a DC path to ground. So, the user must place a resistance R_T , close to the output driver. The

LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in [Figure 20](#).

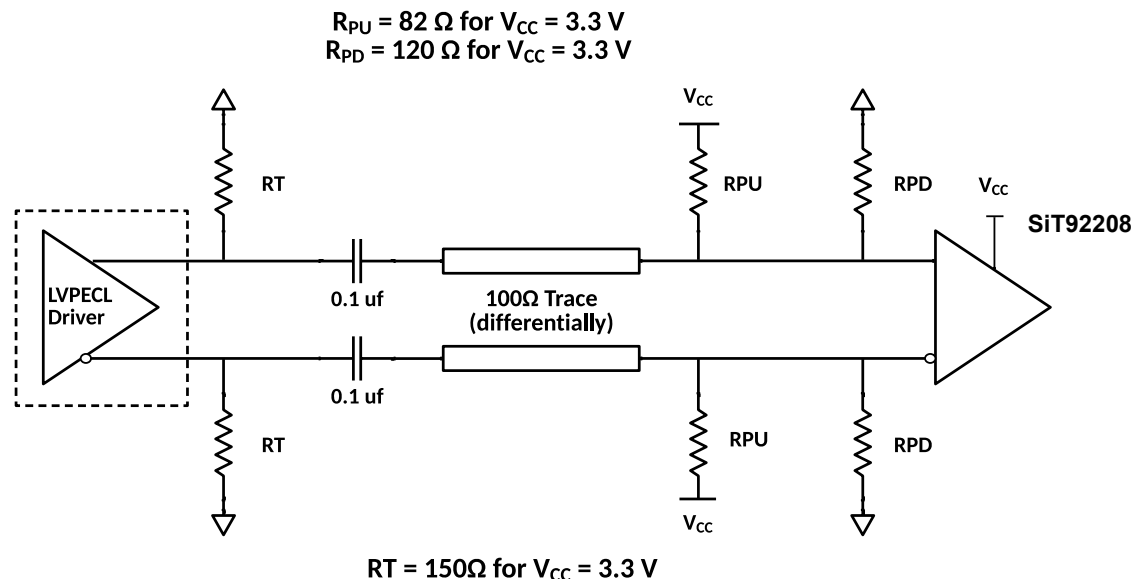


Figure 20. Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance R_{PU} and pull down resistance R_{PD} sets the input common mode voltage for SiT92208. The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{V_{CC} * R_{PD}}{R_{PU} + R_{PD}} = \frac{3.3 * 120}{120 + 82} = 1.961 V$$

The differential input common mode specification of SiT92208 (from data sheet) is $V_{CC} - 1.1 = 2.2 V$, therefore the input common mode set by LVPECL AC coupled termination meets the SiT92208 input common mode

specification. The LVPECL driver chip has resistance R_T providing DC path for the output driver current in the LVPECL driver.

The effective load impedance at the input side of SiT92208 (receiver side) is formed by parallel combination of R_{PU} , R_{PD} .

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7 \Omega$$

Termination of Output Driver of SiT92208 for Various Load Configurations

SiT92208 REF_{OUT} Termination for AC Coupled mode

AC coupling of SiT92208 LVCMOS output driver is shown in Figure 21. We use single termination resistor of 50 Ω to ground. A 0.1 uF AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single 50 Ω resistance to ground. The clock signal is then

AC coupled to the receiver, in this example. C1 is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50 \Omega$$

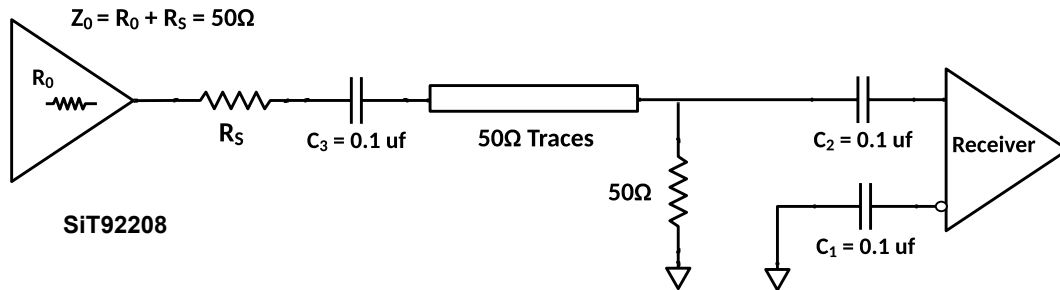


Figure 21. AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

SiT92208 REF_{OUT} Termination for DC Coupled mode

Figure 22 shows how SiT92208 LVCMOS output drive can be terminated to send clock signals in DC coupled mode. The reference voltage V1= V_{CC}/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C₁) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50 \Omega$$

$$\frac{V_{CC} * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{CC}}{2},$$

Typical value of $R_{S1} = R_{S2} = 1 K\Omega$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \Omega,$$

Typical value of $R_{T1} = R_{T2} = 100 \Omega$

$$\frac{V_{CC} * R_{T2}}{R_{T1} + R_{T2}} = \frac{V_{CC}}{2}$$

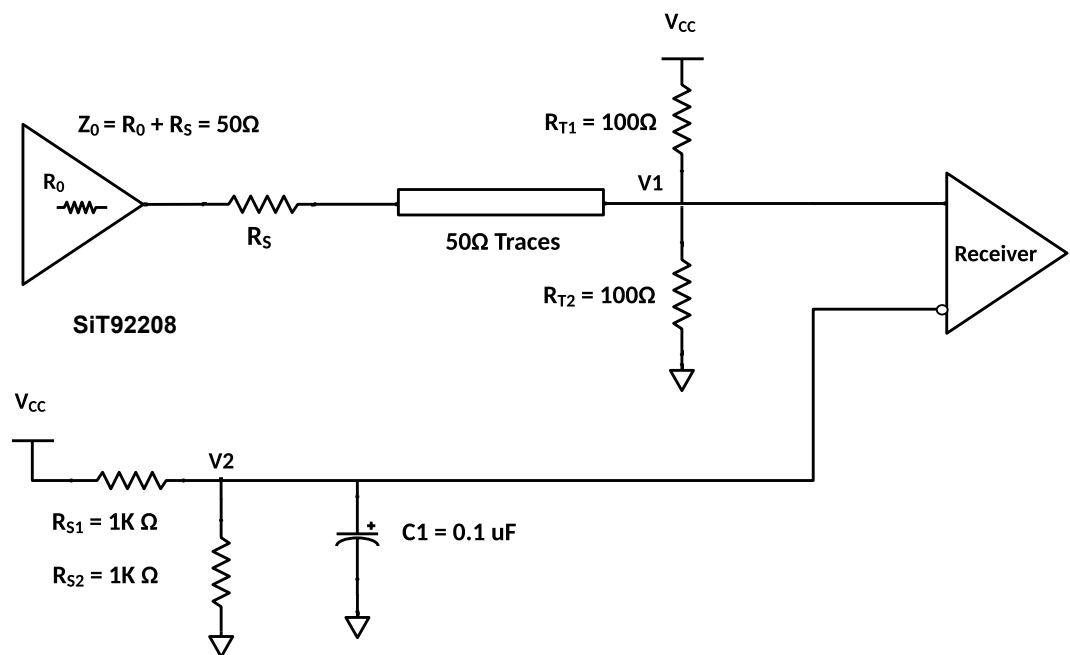


Figure 22. DC coupling of LVCMOS output clock termination – configuration 1

For example, if the SiT92208 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values given below are for when both the single ended swing and V_{CC} are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 23 shows a second input clock configuration where R_{T1} , R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. There will be DC leakage current from SiT92208, for the output termination shown in Figure 23. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 23 is given below

$$Z_o = R_o + R_s = 50 \Omega$$

$$\frac{V_{CC} * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{pp}}{2} = \frac{V_{CC}}{4},$$

$$\text{Typical value of } R_{S1} = 3 K\Omega, R_{S2} = 1 K\Omega$$

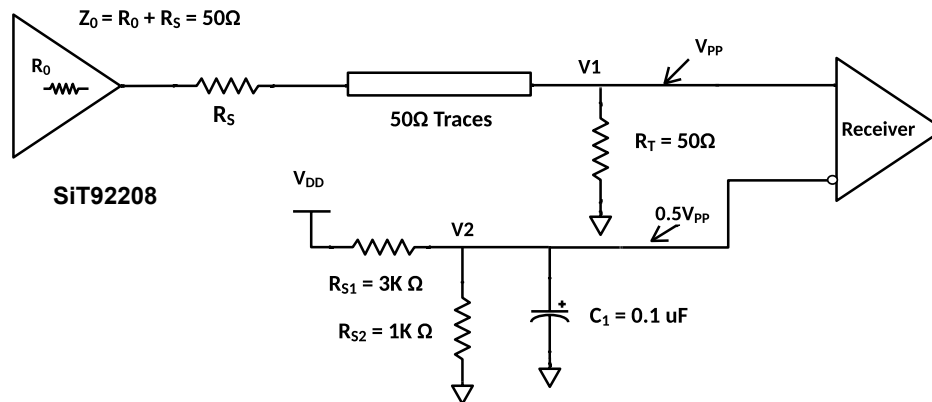


Figure 23. DC coupled LVCMOS output clock configuration – configuration 2

The SiT92208 LVCMOS output driver termination with series RC termination near the buffer is shown in Figure 24. There is a single termination resistor R_T which is connected to ground through a capacitor C_{AC} . The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega}, T_D$$

is the transmission line delay

Typical value for C_{AC} is 60 pF, assuming delay of $T_D = 200$ ps/inch and 5 inch input clock route length.

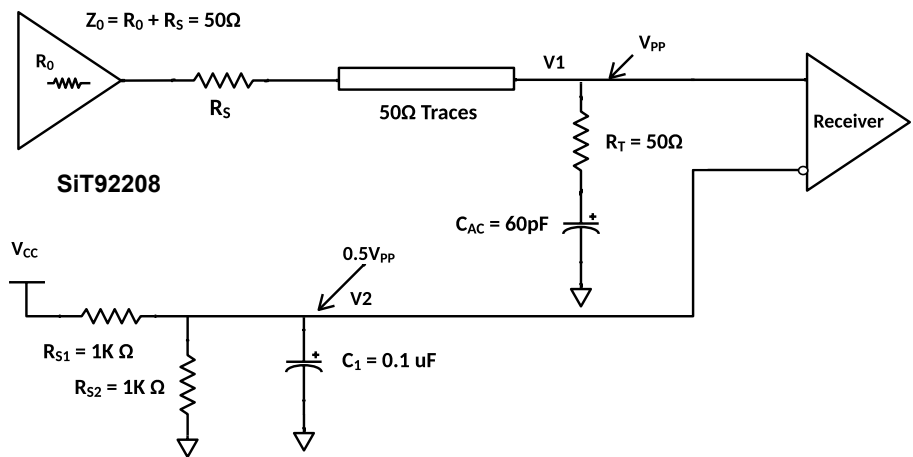


Figure 24. DC coupled LVCMOS output clock with series RC termination – configuration 3

The typical value of R_{S1} and R_{S2} in this case is $1\text{K}\Omega$ and that of C_{AC} is 60pF .

CMOS (Capacitive load)

The capacitive load can be driven as shown in Figure 25 For SiT92208 LVCMOS driver the R_0 is very close to 50Ω by design. Therefore $R_S = 0\Omega$ is recommended.

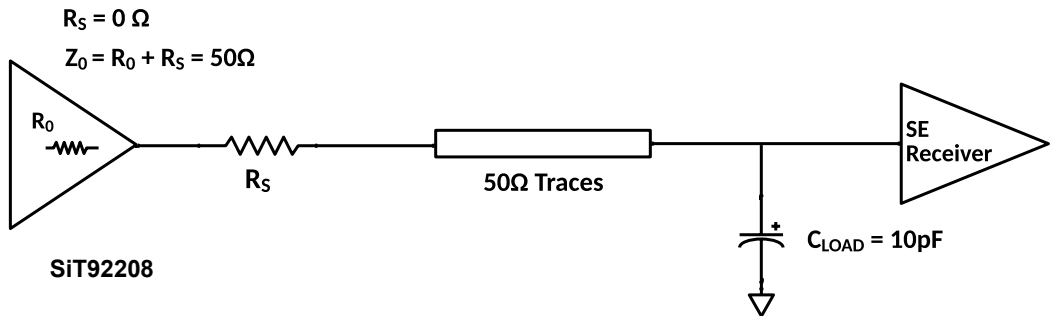


Figure 25. Typical application load

Termination of Output Drivers (DC coupled)

LVDS DC Coupled Output Termination

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in [Figure 26](#).

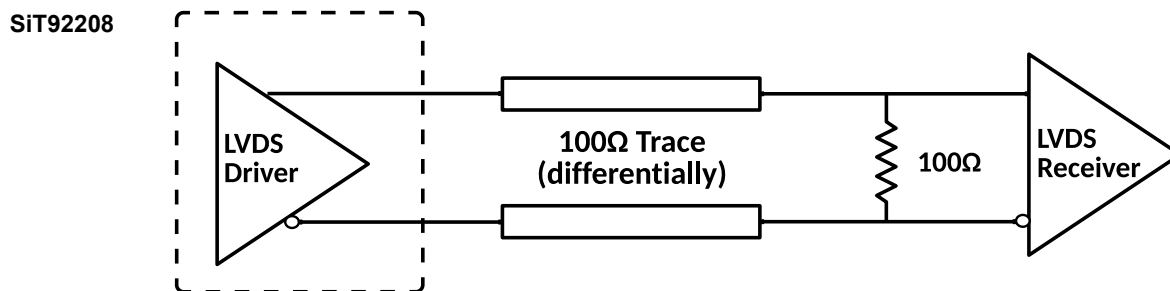


Figure 26. Termination scheme for DC coupled LVDS

HCSL DC Coupled Output Termination

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance R_s is sometimes used to limit the

overshoot during fast transients. The termination scheme is shown in [Figure 27](#).

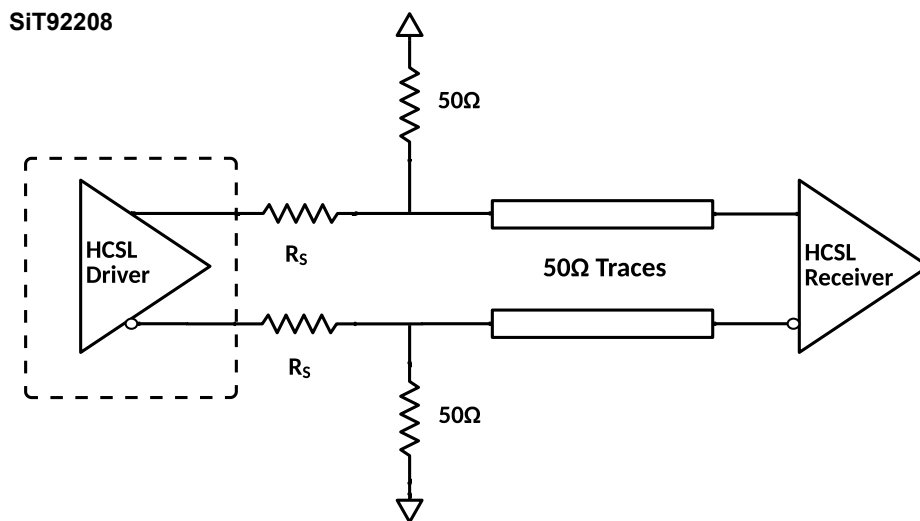


Figure 27. Termination scheme for DC coupled HCSL

LVPECL DC Coupled Output Termination

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source V_{TT} . Typically,

$$V_{TT} = V_{CCO} - 2V.$$

This termination scheme is shown in [Figure 28](#). Alternatively, the user can also implement a Thevenin equivalent of V_{TT} using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in [Figure 29](#).

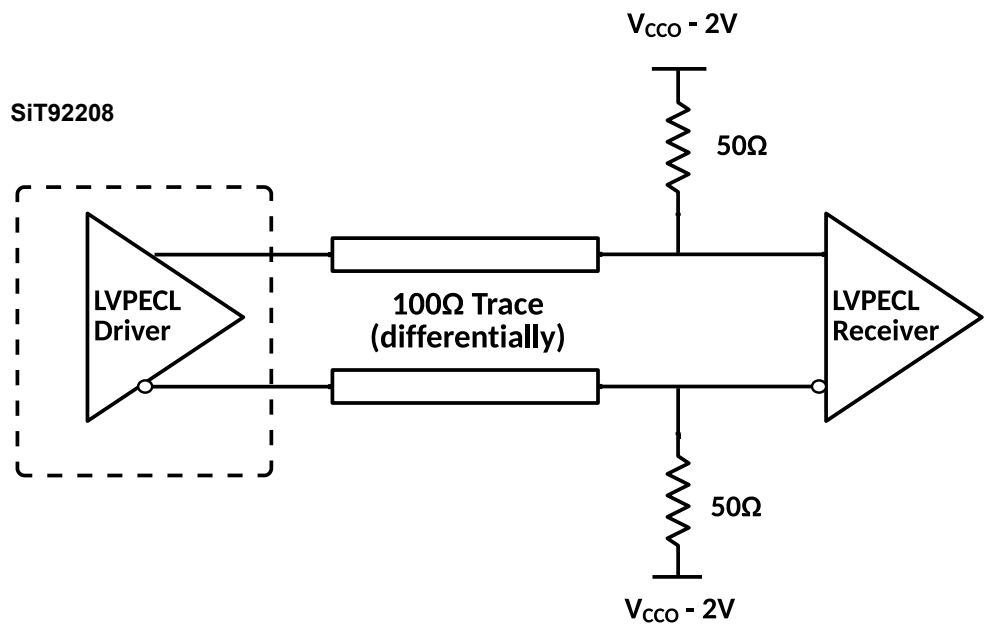


Figure 28. Termination scheme for DC coupled LVPECL

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * V_{CCO}}{R_{PD} + R_{PU}} = V_{CCO} - 2V$$

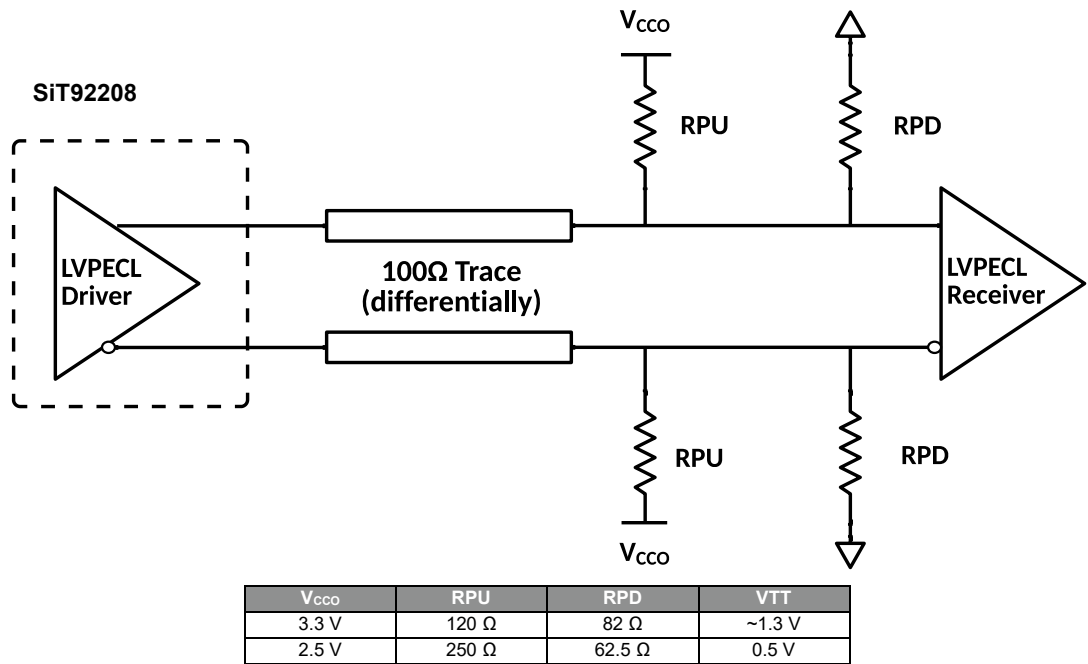


Figure 29. Termination scheme for DC coupled LVPECL, Thevenin equivalent

Termination of Output Drivers (AC coupled) LVDS AC Coupled Output Termination

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 30. First figure shows SiT92208 output driver configured in LVDS mode. The receiver in this case is shown as LVDS

receiver. The second figure shows SiT92208 output driver configured in LVDS mode and the receiver in this case is shown as CML receiver. As long as the LVDS swing is okay with the receiver the AC coupled output termination is same.

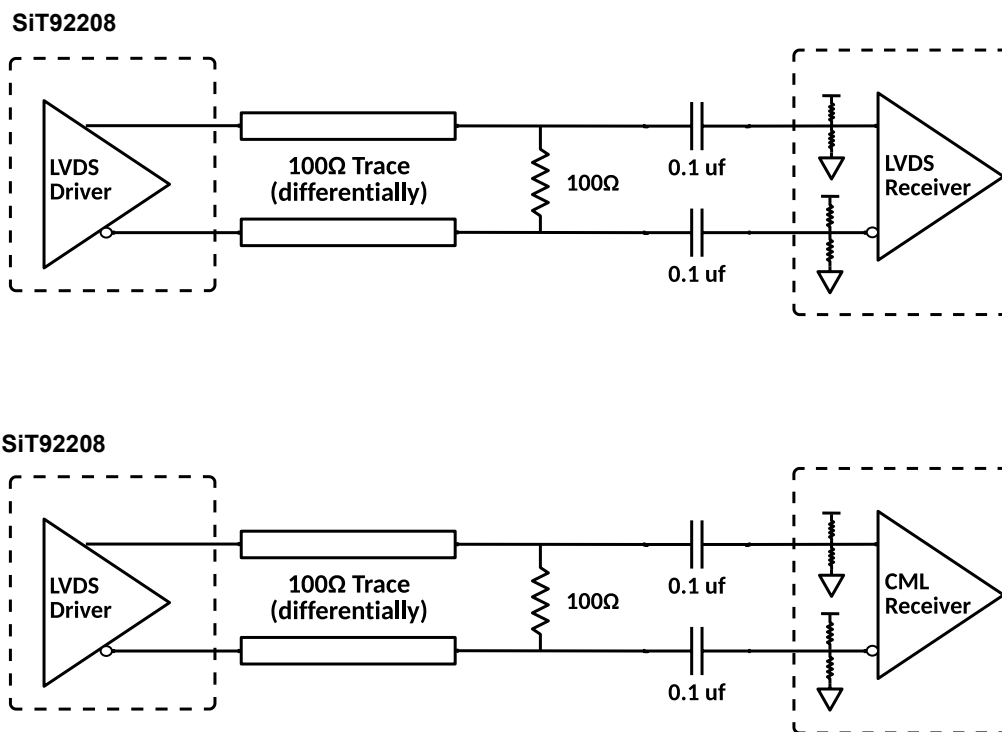


Figure 30. Termination scheme for AC coupled LVDS, driving LVDS receiver and CML receiver

LVPECL AC Coupled Output Termination

The LVPECL should have a DC path to ground. So the user must place a resistance R_T , close to the output driver. The LVPECL AC coupling and Thevenin equivalent V_{TT} termination scheme is shown in Figure 31. SiT92208 swing

reduces by about 20% as the effective load resistor is now the parallel combination of R_T at the driver side and $50\ \Omega$ at the receiver side.

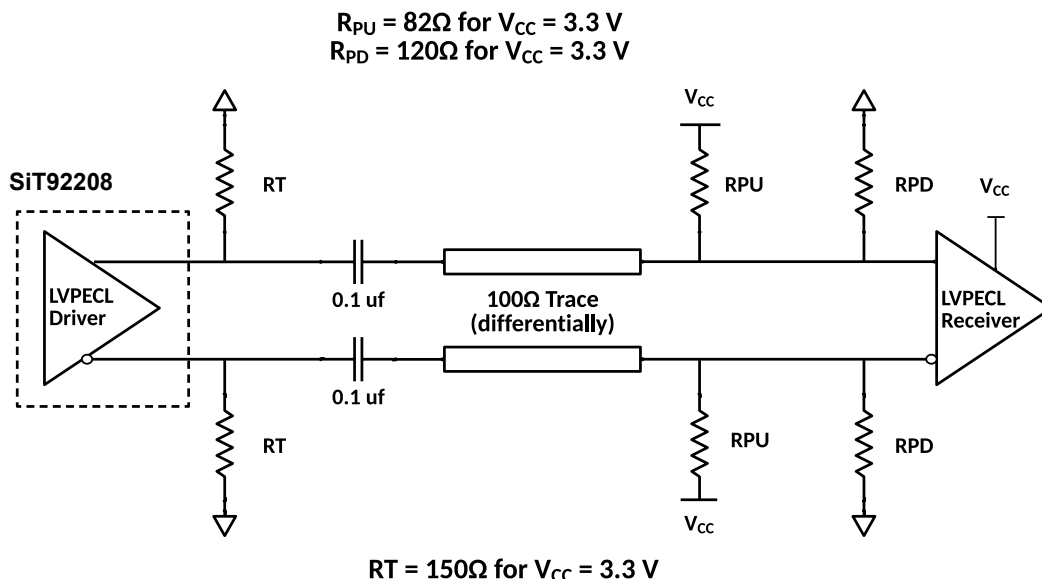


Figure 31. Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance R_{PU} and pull down resistance R_{PD} sets the input common mode voltage for LVPECL receiver. The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{V_{CC} * R_{PD}}{R_{PU} + R_{PD}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The LVPECL driver of SiT92208 has resistance R_T providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the receiver side is formed by parallel combination of R_{PU} , R_{PD} . The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

Termination of Output Drivers in LVPECL Mode, Single Ended, DC coupled

Single ended LVPECL operation is possible. The user can use a balun to convert differential output to single ended output. It is also possible to use the LVPECL driver as one or two separate 700 mV - PP signal. The unused output need to be terminated close to the output driver.

These termination schemes are shown in [Figure 32](#) and [Figure 33](#).

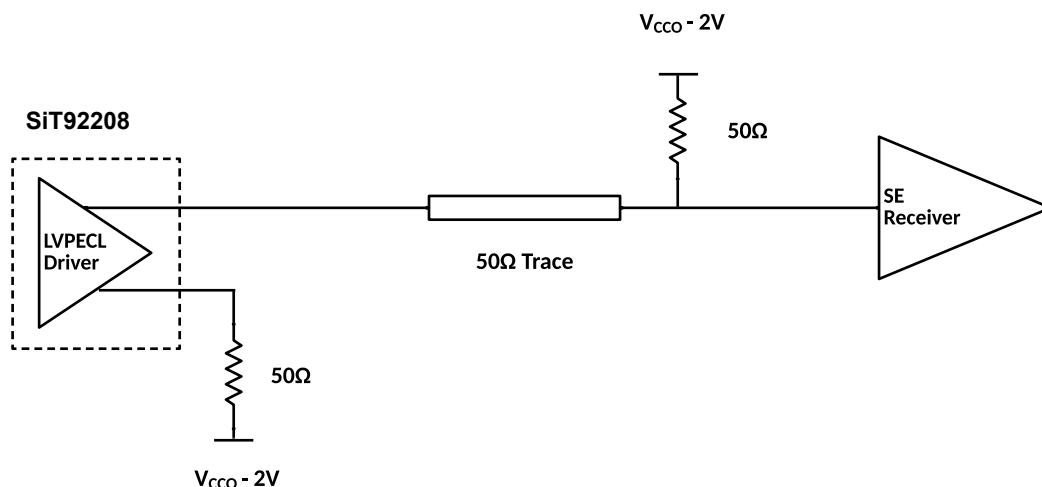


Figure 32. Termination scheme for DC coupled LVPECL, single ended

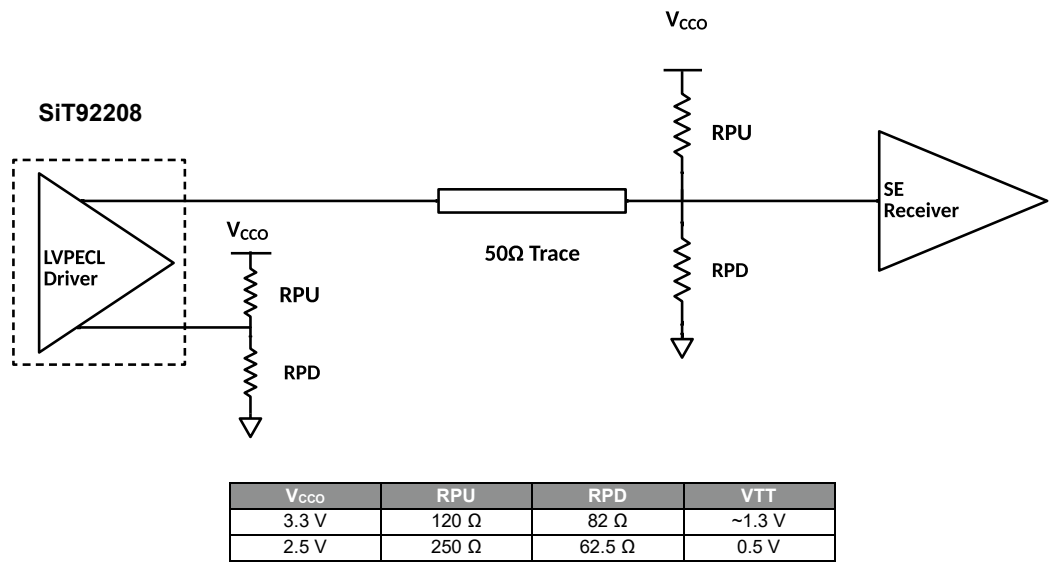


Figure 33. Termination scheme for DC coupled LVPECL, single ended, Thevenin equivalent

Termination of Output Drivers in LVPECL Mode, Single Ended, AC coupled

LVPECL output driver needs a DC path to ground from its output. Therefore 160 Ω (if V_{CC} = 3.3 V) resistor to ground is connected from the output of the LVPECL driver to

ground. If V_{CC} = 2.5 V, the DC path resistance should be 91 Ω. The 50 Ω load termination resistor must be placed close to input receiver and biased to a suitable voltage.

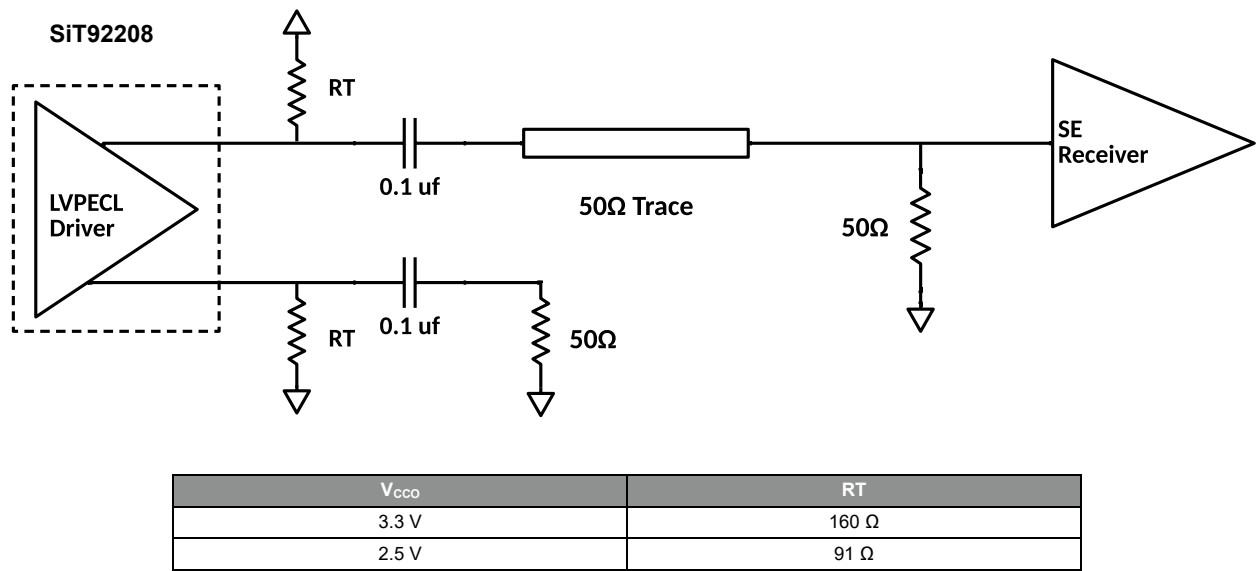


Figure 34. Termination scheme for AC coupled LVPECL, single ended

Termination of Output Drivers in AC coupled HCSL mode

Termination resistor is $50\ \Omega$ to ground, close to the output driver. A series resistance R_S is sometimes used to limit the overshoot during fast transients. AC coupling capacitor of

$0.1\ \mu\text{F}$ is used to couple the output HCSL signal in to the receiver. The same termination can be used for CML receiver.

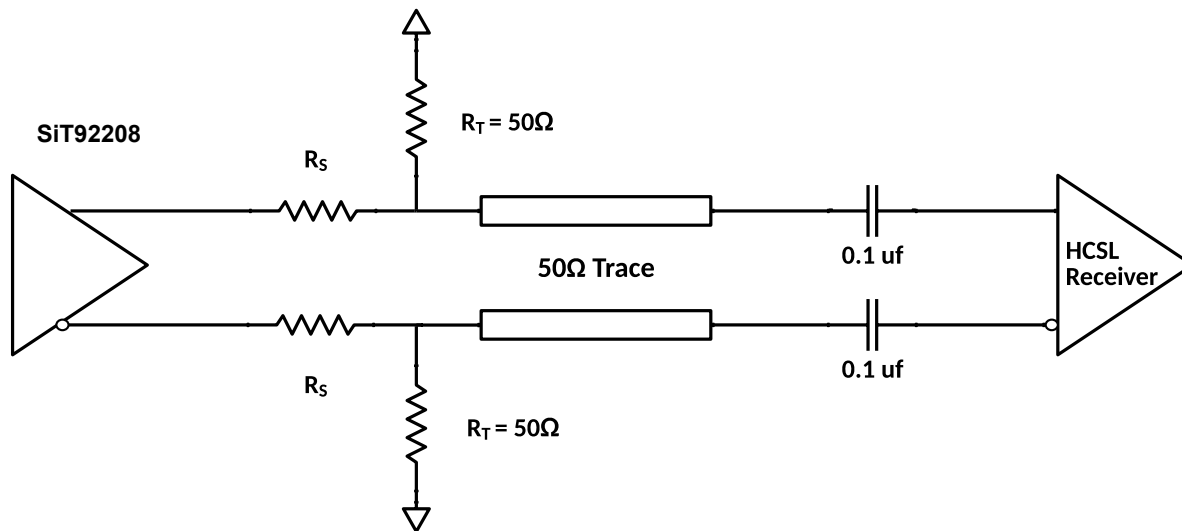


Figure 35. Output driver termination in HCSL AC coupled mode

Thermal Metrics

Table 16. Thermal Metrics

Thermal Metric	SiT92208 QFN 40 pins	Units
θ_{JA} Junction to ambient thermal resistance	31.7	°C/W
θ_{JB} Junction to board thermal resistance	3.60	°C/W
θ_{JC} Junction to case thermal resistance	29.6	°C/W
ψ_{JT} Junction to top characterization parameter	1.07	°C/W

HOT Swap Recommendations

Introduction

Hot-swap is a term used to refer to the insertion and removal of a daughter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can be damaged.

Typical Differential Input Clock

For example, Figure 36 shows a typical LVPECL driver and differential input. If the power of the driver (V_{CCO}) is turned on before the input supply (V_{CCI}), there is a possibility that the input current could exceed the limit and damage diode D1.

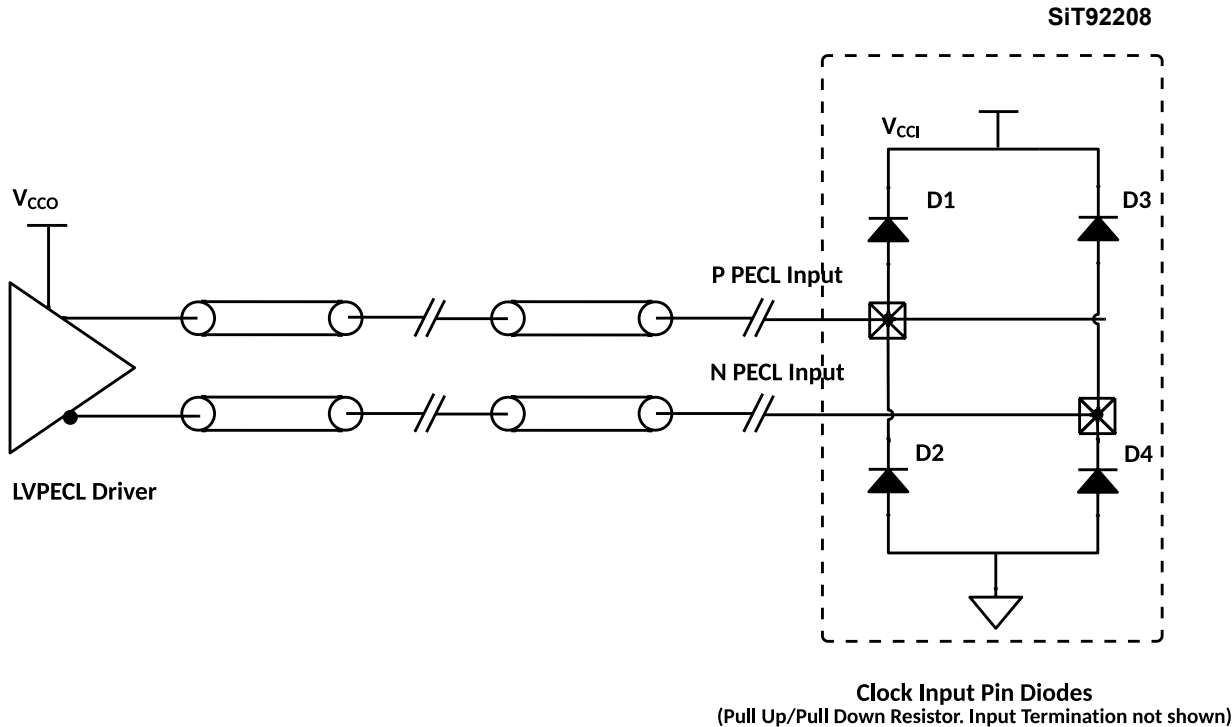


Figure 36. Typical input differential clock

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though it's not necessary, but if board space allows, some of the

examples have an optional 100 pf capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible.

Input Clock Termination with Hot Swap Protection

LVPECL Termination Example

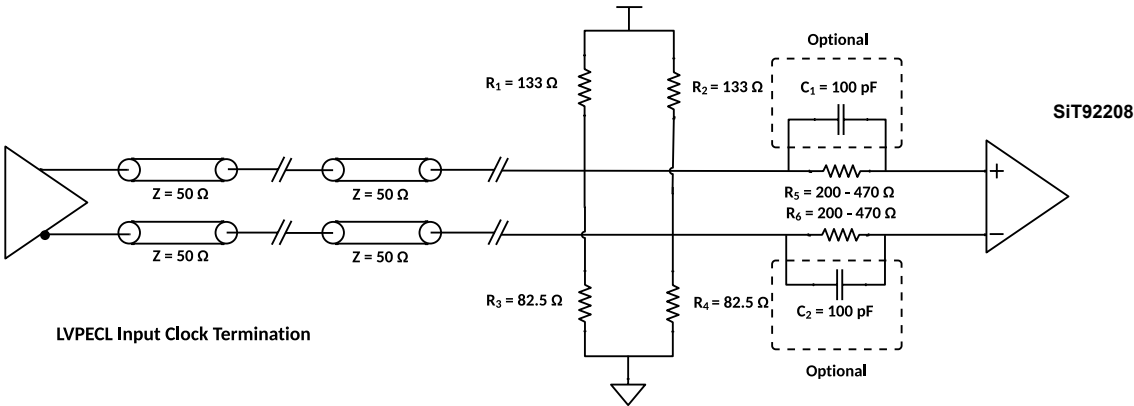


Figure 37. LVPECL termination with hot swap protection

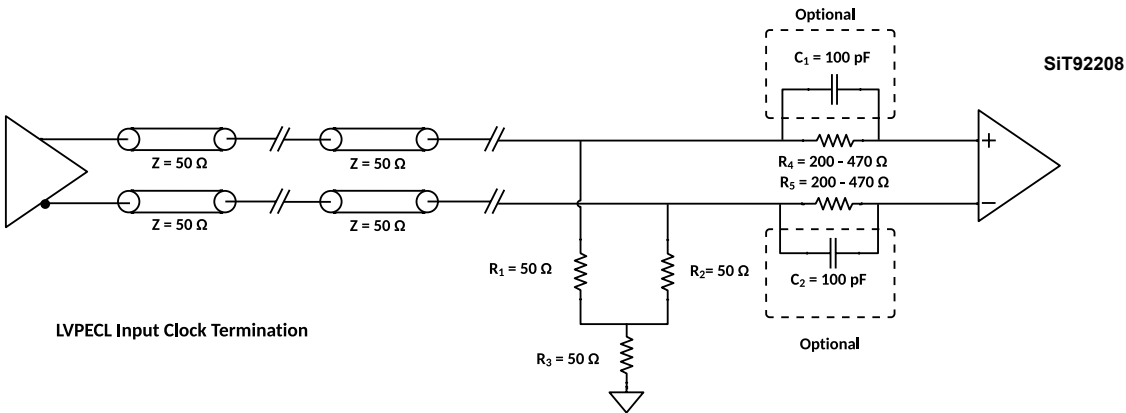


Figure 38. LVPECL termination with hot swap protection

LVDS Input Clock Termination Example

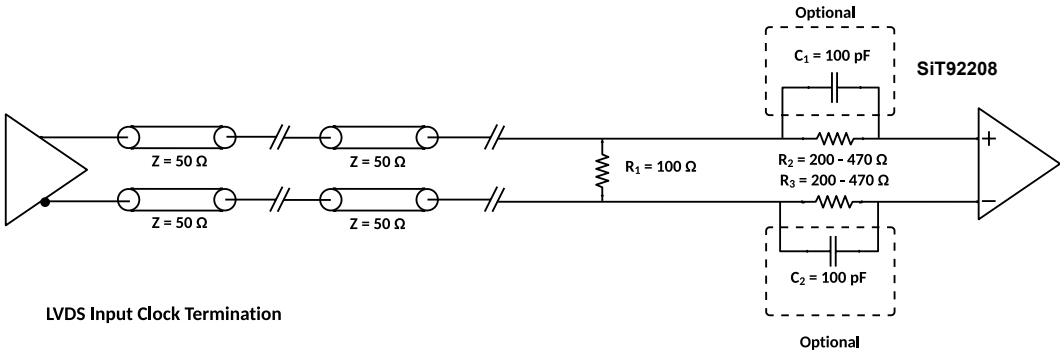


Figure 39. LVDS termination with hot swap protection

HCSL Input Clock Termination Example

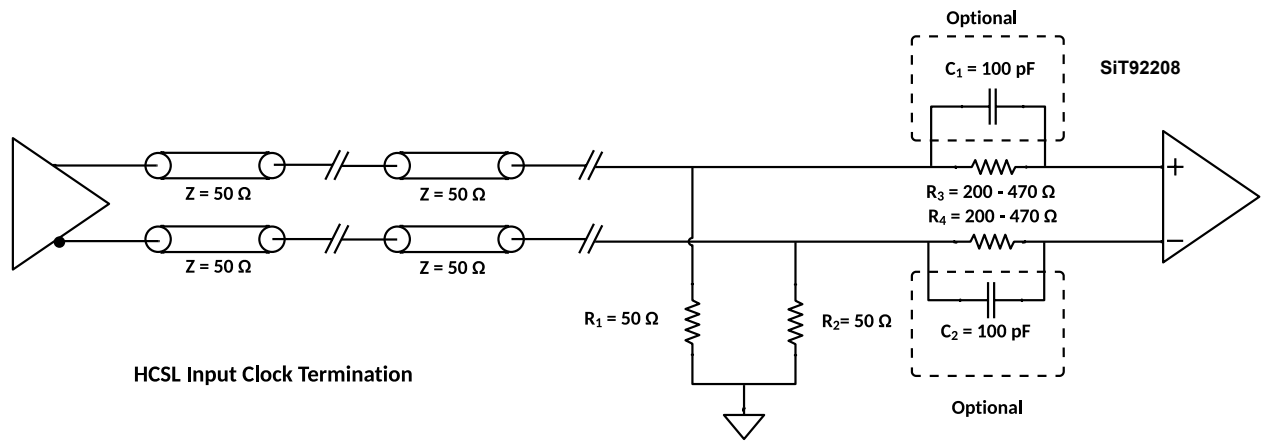


Figure 40. HCSL termination with hot swap protection

LVC MOS Input Clock Termination with Hot Swap Protection

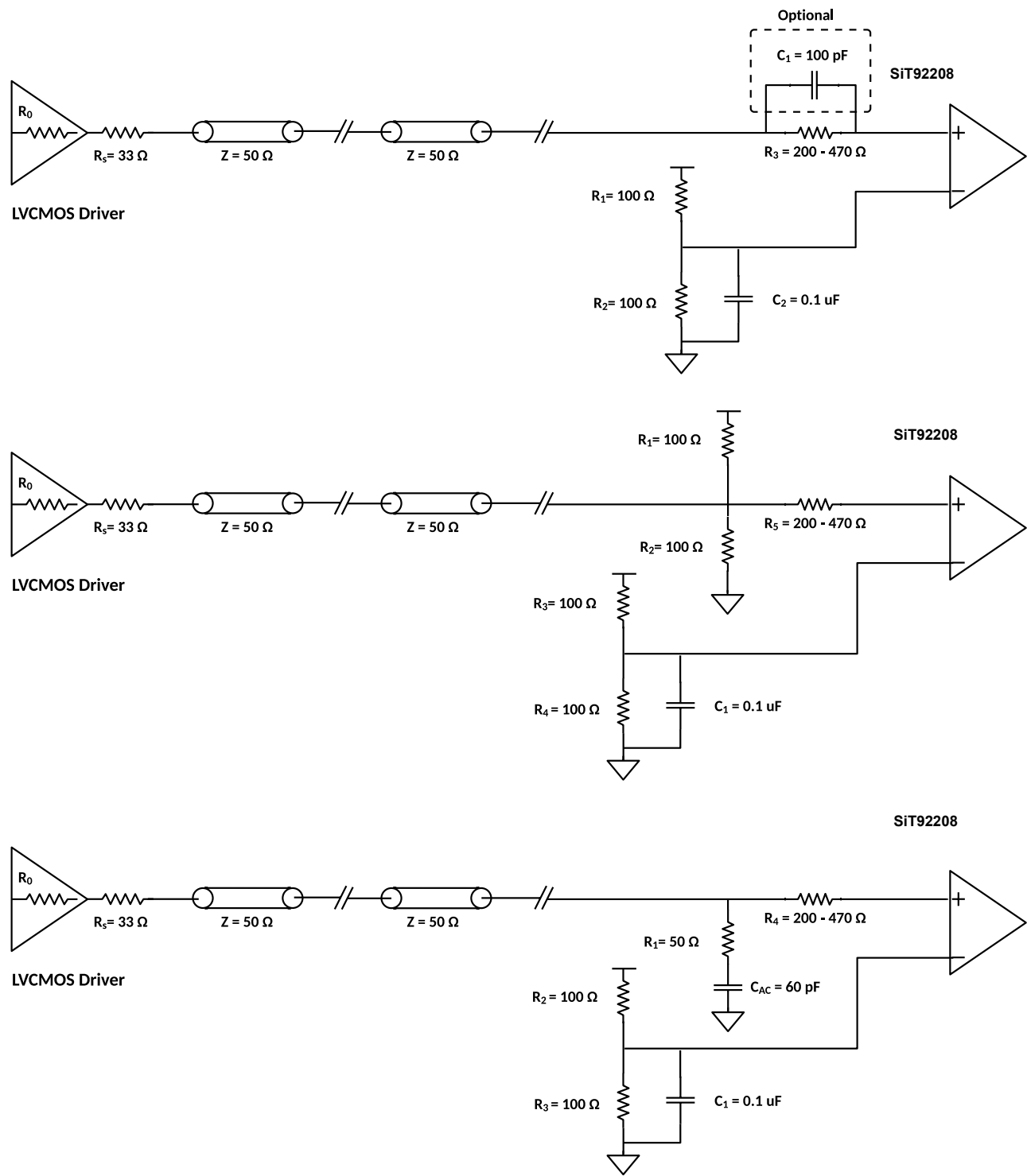


Figure 41. LVC MOS input clock termination with hot swap protection

LVC MOS Output Clock Termination with Hot Swap Protection

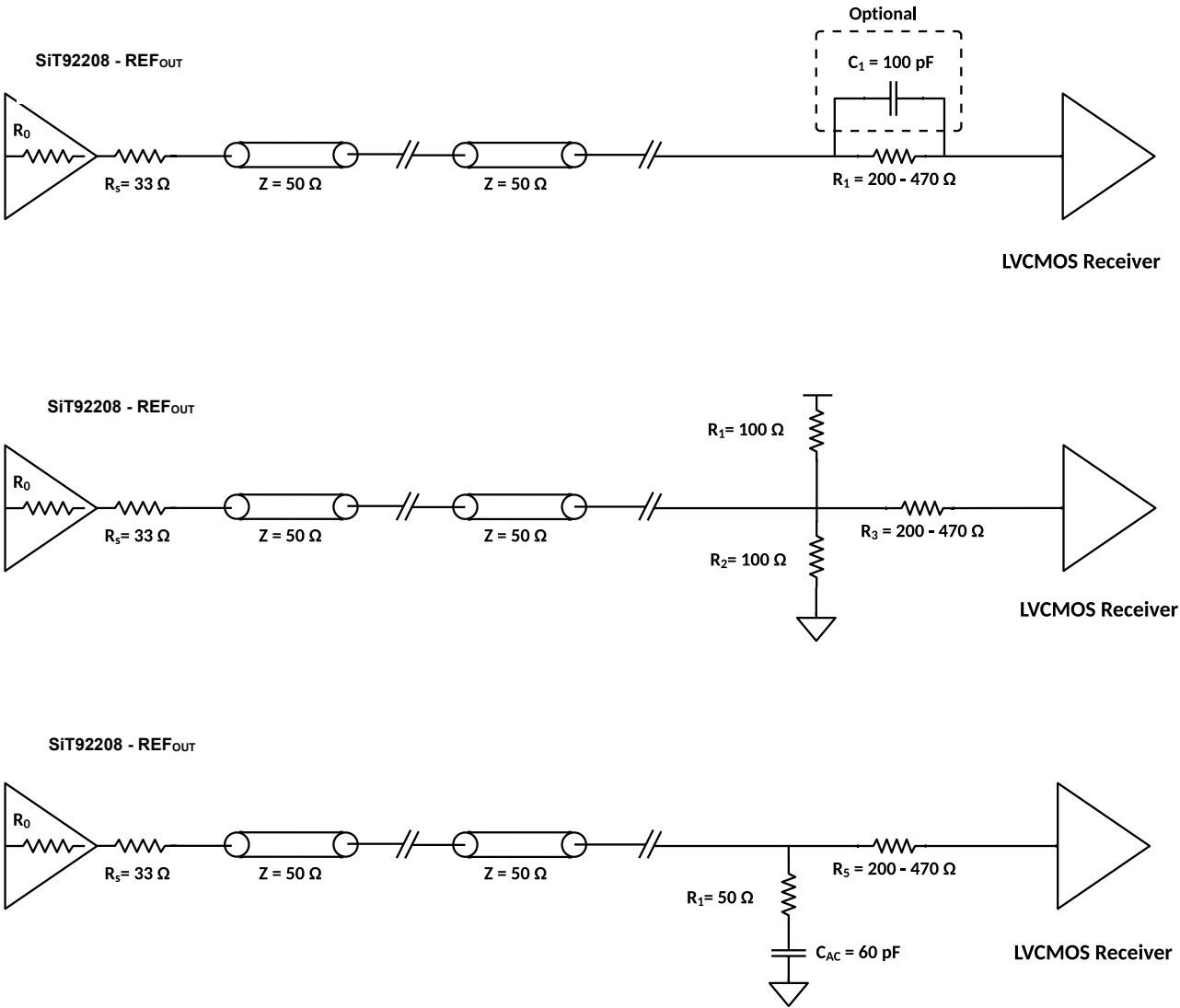


Figure 42. Different types of LVC MOS output clock termination with hot swap protection.

Parameter Measurement Information

Differential Input Level

The parameter definitions related to differential input level is shown in Figure 43.

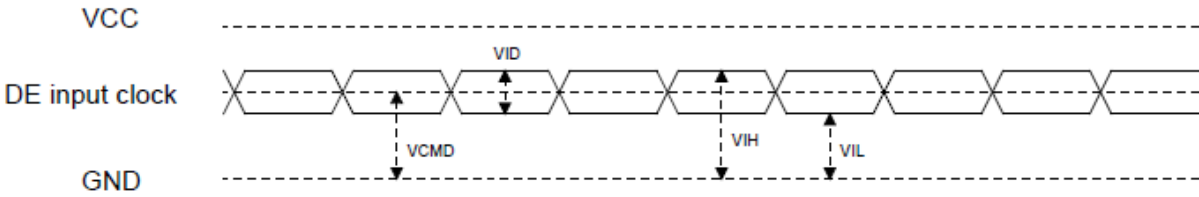


Figure 43. Parameters related to differential input level

Differential Output Level

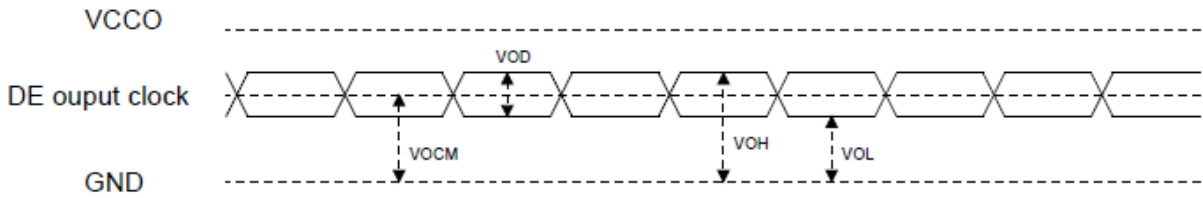


Figure 44. Parameters related to differential output clock levels

Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown in Figure 45.

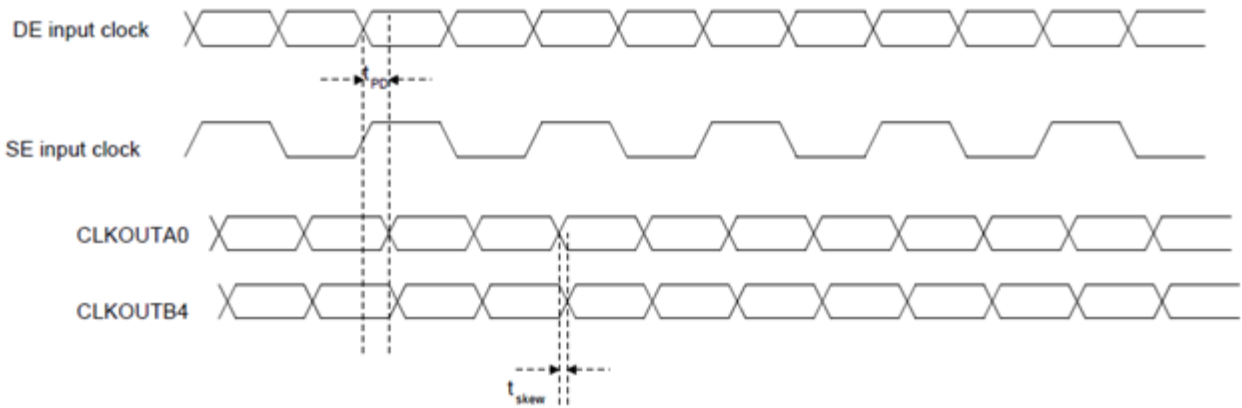


Figure 45. Parameter definitions of propagation delay and skew

Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown in Figure 46.

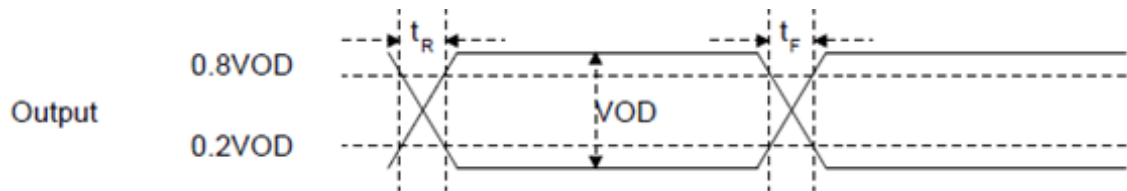


Figure 46. Parameter definitions related to rise and fall times

Isolation

Isolation is a measure of the coupling of clock toggling in unselected input clock path on the output clock. Let us say that CLOCK0 path is selected and there the clock frequency is 156.5 MHz at 0 dBm power. If a clock is toggling in

CLOCK1 path at 156 MHz at 0 dBm, then we there may be a tone at an offset of 0.5 MHz from the carrier, in the output clock. The power of this tone with respect to the carrier is called isolation.

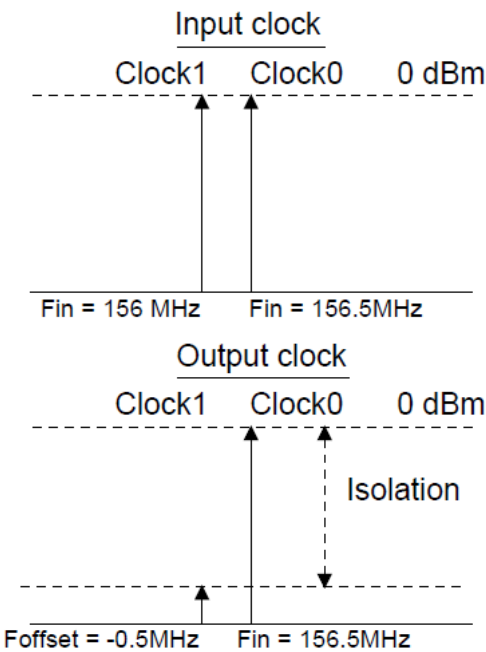


Figure 47. Parameter definition of isolation

Operation in Multiple V_{CCO} Supply Domains

The V_{CCOA} pins, 3 and 6 on the left side are shorted internally. These pins along with ODR CLK_{OUT}A0 to CLK_{OUT}A3 belong to a single supply domain. The V_{CCOB} pins, 25 and 28 on the right side are shorted internally. These pins along with ODR CLK_{OUT}B0 to CLK_{OUT}B3 belong

to a single supply domain. These two supply domains are totally independent of each other. Pin 3, 6 can be connected to say 3.3 V while pin 25, 28 can be connected to 2.5 V. In this example, CLK_{OUT}A0 to CLK_{OUT}A3 will be 3.3 V output driver. CLK_{OUT}B0 to CLK_{OUT}B3 will be 2.5 V output driver.

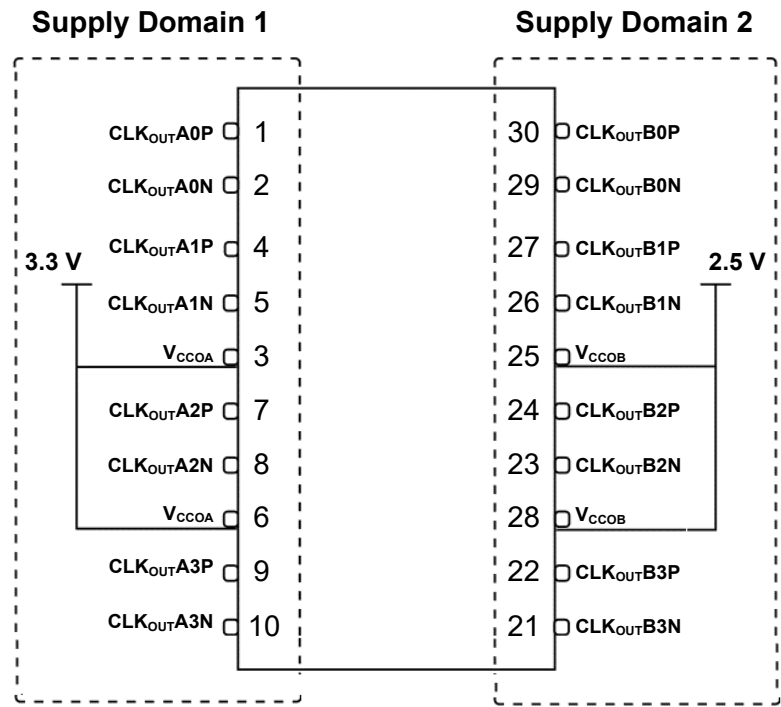
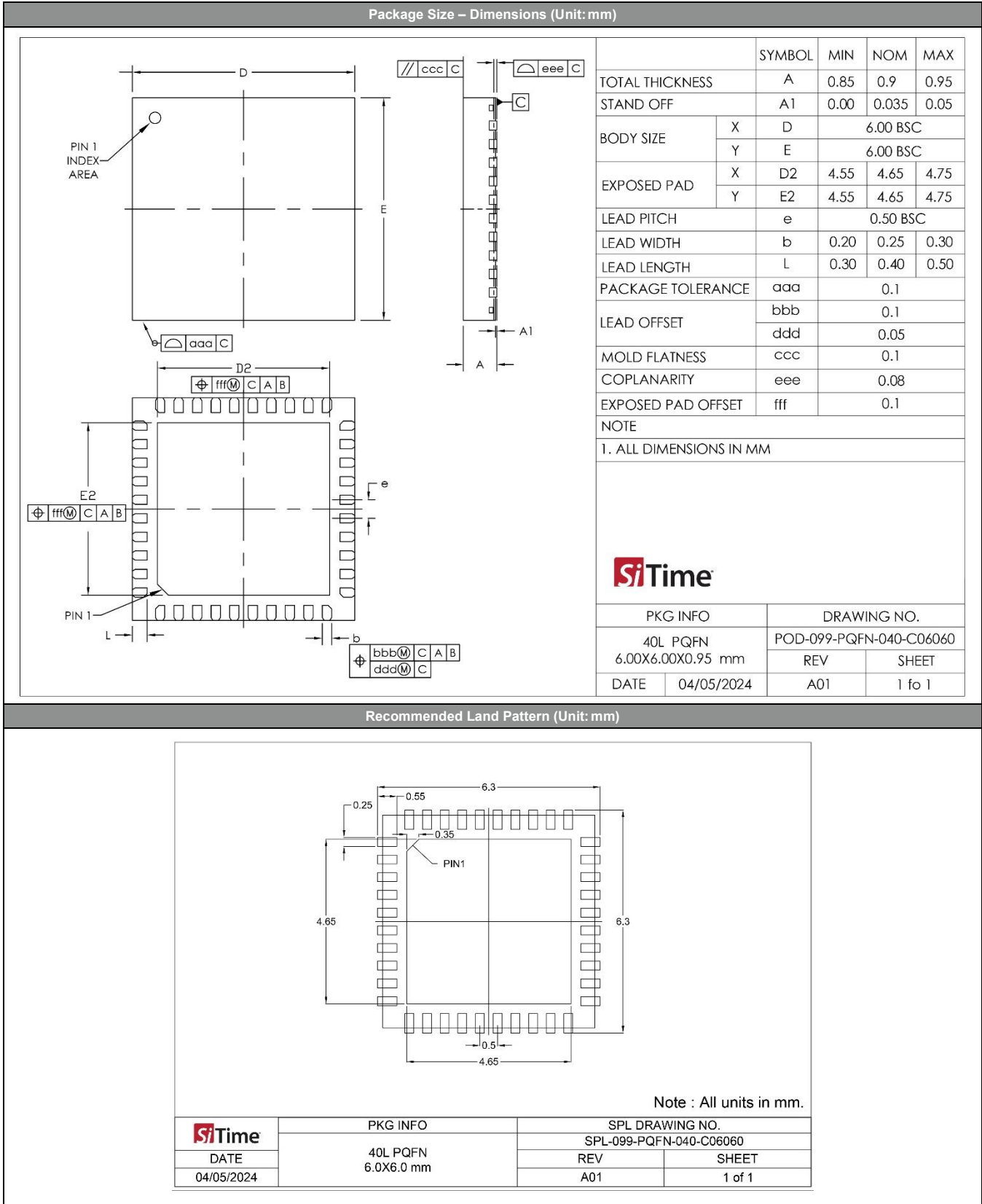
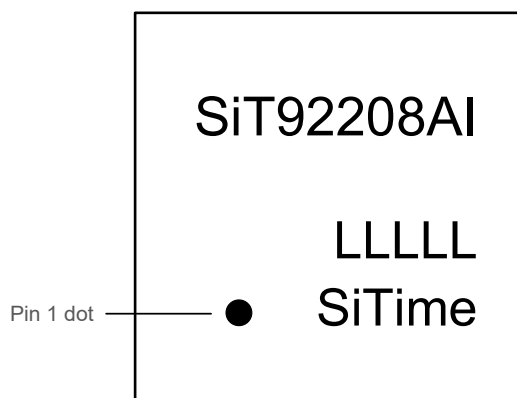


Figure 48. Multi Supply operation of SiT92208

Package Dimensions and Patterns



Top Marking



Line 1: "SiT92208AI", SiTime part number
Line 2: Blank
Line 3: "LLLLL", Lot code from SiTime
Line 4: Pin 1 dot and "SiTime" logo

Thermal Management

SiT92208 has an exposed pad (EPAD) on the package to provide the means for thermal relief and excellent grounding. A land pattern must be incorporated on the circuit board as detailed in the package drawing; additional guidelines listed below:

- Minimal number of thermal vias: 9
- Minimal plating thickness of thermal vias: 25 μm
- Minimal thermal via diameter: 0.3 mm (can be smaller for larger number of vias)
- Minimal combined thickness of ground plane(s): 35 μm (1 oz)
- Thermal vias should be directly under the EPAD
- Thermal vias should be through holes
- Thermal vias should be connected around their entire circumference with all ground plane(s)
- Essentially, it is recommended to have a board design that has equal or better thermal dissipation than the JESD51-5 board

Revision History

Table 17. Revision History

Revisions	Release Date	Change Summary
0.5	15-Apr-2024	Initial Release
0.51	8-Jul-2024	Ordering Information update
0.52	11-Feb-2025	Added Pin Configuration; Top Marking section
0.53	12-Feb-2025	Ordering Code for Packaging updated with 4Ku/reel code "P"
0.54	5-May-2025	Ordering Code for Packaging updated with 4Ku/reel code "P" and 500u/reel code "N"
0.55	16-Sep-2025	Fixed Figure 2. SiT92208 Pin Configuration Top View
1.0	22-Jun-2026	Top marking updated; Production version release Max additive Jitter and output skew specs updated
1.1	17-Sep-2026	LVDS output differential peak voltage conditions and specs updated

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