Chorus SiT91211

Low Phase Noise MEMS Clock Generator

Description

The Chorus SiT91211 is a low phase noise MEMS-based clock generator designed for low-power, low jitter applications. The device has a single clock domain and can drive up to 8 low-skew single-ended output loads or 4 low-skew differential loads.

The Chorus SiT91211 integrates an internal MEMS resonator as the frequency source for the internal PLL, eliminating the need for an external oscillator or resonator. The integrated MEMS improves system reliability by eliminating traditional clock generator's requirements for an external quartz and along with it, issues like activity dips due to shock and vibration and matching requirements.

The device is fully configurable in output frequency, clock output buffer type (differential and LVCMOS) and individual output enables, through the serial interface. Internal monitor flags and alarm conditions can be configured to be reported through GPIOs.

The device is compliant with PCIe Generation 1-7 including configurable spread-spectrum clocking.

User-defined, pre-programmed, and user-programmable NVM enables a high degree of flexibility and defined startup-configuration. Configurable GPIO pins support state changes such as individual output enable selection.

Features

- Standard Frequencies from 1 MHz to 700 MHz
- Fully integrated MEMS-based clock source
- Configurable clock domain and 4 differential outputs or 8 single-ended outputs
- Configurable output clock drivers:
  - LVDS, HCSL, LVPECL, LVCMOS
- Excellent frequency stability
  - ±20 ppm (-40°C to 105°C)
  - ±50 ppm (-40°C to 105°C)
- Configurable spread-spectrum clock generation
- Compliant with PCIe Generation 1 to 7
- Clock fault monitors (Lock Loss)
- Supply voltage of 1.8 V to 3.3 V
- Low phase jitter, 200 fs maximum (12 kHz-20 MHz)
- Resistant to shock/vibration
- Max. Operating range: -40°C to 105°C
- I²C or SPI serial interface for configuration
- QFN 24 pin 4 x 4 mm, 0.5 mm pitch (wettable flank) package

Applications

- Datacenter, Switches, Smart NIC
- Wireless 5G infrastructure equipment
- High Speed Links: Ethernet, Optical
- High Speed Interconnect: PCIe and SerDes

Order samples

Block Diagram

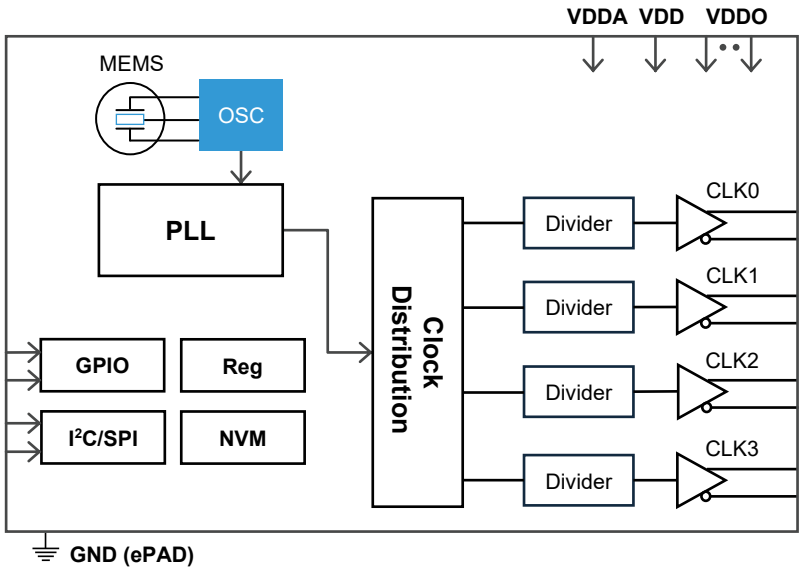

Figure 1. Chorus SiT91211 Block Diagram

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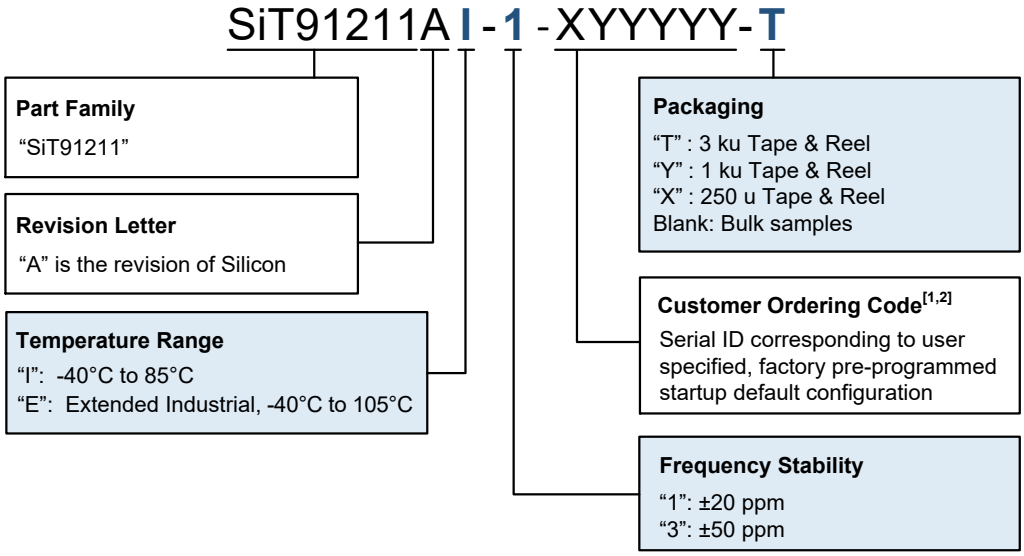
Ordering Information



Notes:

1. X = "A" and "B" customer device, "C to "Z" reserved.
   A: Denotes blank devices.
   B: Denotes Pre-configured devices, contact SiTime for the specifics.
2. Y = 0...9, A…Z for custom serial ID.

Functional Description

The Chorus SiT91211 is a commercial grade, low-jitter clock generator with an integrated SiTime MEMS resonator targeting applications in the Communications, Enterprise and Industrial segments. The can provide 4 configurable differential or 8 single-ended low skew outputs, or a combination of both. Differential outputs can be configured up to a maximum clock frequency of 700 MHz, while single ended outputs can be configured up to a maximum clock frequency of 220 MHz. The integrated MEMS resonator enables the Chorus SiT91211 to be operated without an external quartz crystal or oscillator reference, thereby eliminating the need for associated matching requirements.

The output drivers support commonly used signal formats, such as LVPECL, LVDS, HCSL, LVCMOS, as well as FlexSwing. Individual VDDO pins, capable of accepting between 1.8 V and 3.3 V, are available for each differential output driver, The core voltage supply (VDD, VDDA) accepts 3.3 V, 2.5 V, or 1.8 V and is independent from the output supplies (VDDO).

The SiT91211 combines SiTime's highly reliable MEMS resonator with a wideband PLL, on-chip temperature compensation, and four integer dividers to generate high-performance outputs with typical jitter of 150 fs and frequency stability of ±20 ppm or ±50 ppm across the wide temperature range, -40°C to 105°C. The Chorus SiT91211's on-chip regulators ensure extremely good power supply noise rejection, ensuring minimal deviation from the jitter specification due to power supply noise. Spread spectrum modulation is available in the SiT91211, to help reduce electromagnetic interference (EMI) by spreading output clock energy over a broader range.

The elimination of an external reference clock source leads to improved ease of use by eliminating the need for any matching or frequency jump issues. Importantly for mission critical applications, all dependence on quartz crystals (which have been shown to be prone to high failure rates) is eliminated. In addition to improved failure rates, internal functions such as the MEMS reference clock, bandgap reference, PLL, and VDDOs, and output drivers are monitored. This is a significant improvement over common on-chip status monitors in clock generator chips. Fault conditions on these monitored functions can be configured to be sent out to GPIO outputs individually or as a combined alarm signal or read via I^2C or SPI interface. This allows an external MCU to be alerted to a fault condition in the clock generator to take appropriate action consistent with system requirements.

The SiT91211 is available optionally with or without a serial interface (I^2C or SPI). The serial interface can be used to read internal registers, including status of the internal monitoring functions. A user can use In-System Configuration (ISC) mode to write to contents of internal registers to modify the device configuration via the serial interface. In such a use case, the modified configuration will be lost at the next power cycle. The SiT91211 allows the user to burn the new configuration into the NVM via the In-System Programming (ISP) Mode, which will then be the new default configuration at the next power cycle.

Optionally, the user can store up to four different static clock configurations in the SiT91211 NVM, one of which is selectable at power-up based on the status sampled on the two Frequency Select pins. The four static configurations cannot be modified using ISP mode, but ISC mode can still be used to modify internal register contents.

For applications which require only a standard configuration, the SiT91211 is also available as a factory configured device without a serial interface, which allows the use of the serial interface pins as additional GPIOs. SiTime will program the NVM to configure the devices according to specific customer requirements.

The SiT91211 also supports Digitally Controlled Oscillator (DCO) Mode in which the user can modulate the output frequencies via serial interface (I2C/SPI). The user can control two registers which modulate the internal Voltage Controlled Oscillator (VCO) in the PLL. All enabled outputs will change simultaneously in response to the VCO update. The VCO tuning range is ±800 ppm with an increment or decrement step size of 0.023 ppt. This can be achieved by writing to a 36-bit DCO tuning register. A second 20-bit register allows the user to limit or clip the tuning range to less than ±800 ppm. The clipped tuning range can be set with a step size of 0.753 ppb.

Chip Status Monitoring

The SiT91211 monitors multiple internal parameters and makes these status monitoring functions available to an external MCU via GPIO pins or through direct access of internal registers via I²C/SPI. All the status signals listed in the table below are also accessible via register reads over the serial interface (I²C or SPI).

Table 1. Status Monitoring Signals

Monitoring Function	Monitored on GPIO Pin (Parts without I²C/SPI)	Monitored on GPIO Pin (Parts with I²C/SPI)	Function
MEMS Clock Monitor	Pin 2 / 3 / 4 / 6 / 7 / 23 / 24	Pin 2 / 3 / 23 / 24	Goes low when internal MEMS clock does not oscillate
Bandgap Monitor	Pin 2 / 3 / 4 / 6 / 7 / 23 / 24	Pin 2 / 3 / 23 / 24	Goes low when internal band gap reference falls below threshold
PLL Lock Monitor	Pin 2 / 3 / 4 / 6 / 7 / 23 / 24	Pin 2 / 3 / 23 / 24	Goes low when PLL loses lock with MEMS reference clock
Clock0 Ready	Pin 2	Pin 2	Goes low when Clock0 driver is not toggling / has a fault
Clock1 Ready	Pin 3	Pin 3	Goes low when Clock1 driver is not toggling / has a fault
Clock2 Ready	Pin 23	Pin 23	Goes low when Clock2 driver is not toggling / has a fault
Clock3 Ready	Pin 24	Pin 24	Goes low when Clock3 driver is not toggling / has a fault
Clock01 Ready	Pin 6	-	Goes low when Clock0 or Clock1 driver are not toggling / have a fault
Clock23 Ready	Pin 7	-	Goes low when Clock2 or Clock3 driver are not toggling / have a fault
VDDO0 Good	Pin 2	Pin 2	Goes low when VDDO0 supply is below NVM-configured threshold
VDDO1 Good	Pin 3	Pin 3	Goes low when VDDO1 supply is below NVM-configured threshold
VDDO2 Good	Pin 23	Pin 23	Goes low when VDDO2 supply is below NVM-configured threshold
VDDO3 Good	Pin 24	Pin 24	Goes low when VDDO3 supply is below NVM-configured threshold
All Clocks Ready	Pin 2 / 3 / 4 / 6 / 7 / 23 / 24	Pin 2 / 3 / 23 / 24	Goes low when any enabled clock output is not toggling / has a fault
Alarm_B	Pin 2 / 3 / 4 / 6 / 7 / 23 / 24	Pin 2 / 3 / 23 / 24	Goes low when any fault is triggered
ISP_Burn_Success	Pin 4	(Access via register read)	Asserted when in-system NVM burn is successful
VDDO01 Good	Pin 6	-	Goes low when VDDO0 or VDDO1 are below NVM-configured thresholds
VDDO23 Good	Pin 7	-	Goes low when VDDO2 or VDDO3 are below NVM-configured thresholds
Die Temperature Out of Range	Accessible via register reads only		Asserted if die temperature is outside user configured range. Available via direct register access through I²C/SPI

General Purpose Inputs

Table 2. User Configurable Input Signals[3]

Input Function	Available on GPIO Pin (Parts without I²C/SPI)	Available on GPIO Pin (Parts with I²C)	Available on GPIO Pin (Parts with SPI)	Function
SSEN / $\overline{\text{SSEN}}$	Pin 1 / 3 / 4 / 8	Pin 1 / 3 / 4	Pin 1 / 3	Spread Spectrum enabled on all outputs (configurable active high or low)
OE0 / $\overline{\text{OE0}}$	Pin 2 / 3	Pin 2 / 3	Pin 2 / 3	Enable Output 0 (configurable active high or low)
OE1 / $\overline{\text{OE1}}$	Pin 2 / 3	Pin 2 / 3	Pin 2 / 3	Enable Output 1 (configurable active high or low)
OE2 / $\overline{\text{OE2}}$	Pin 1 / 6 / 7	Pin 1 / 6 / 7	Pin 1 / 6	Enable Output 2 (configurable active high or low)
OE3 / $\overline{\text{OE3}}$	Pin 1 / 6 / 7	Pin 1 / 6 / 7	Pin 1 / 6	Enable Output 3 (configurable active high or low)
OE_all / $\overline{\text{OE\_all}}$	Pin 2 / 7	Pin 2 / 7	Pin 2	Enable all Outputs (configurable active high or low)
FS0	Pin 9 / 23	Pin 23	Pin 23	Frequency Select 0
FS1	Pin 8 / 24	Pin 24	Pin 24	Frequency Select 1

Note:

3. The I²C and SPI pins can be reconfigured, in factory, as GPIO pins. Such parts (without the I²C or SPI interface) can be ordered directly only from SiTime.

Power Supply Sequencing

The core power supplies (VDDA and VDD) are required to be at the same voltage. VDDOx can be chosen independently as required by the clock receiver. All VDDOx can be sequenced independently of each other and VDD/VDDA. However, VDD and VDDA should be brought up together.

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage. See Test Circuit Diagrams for the test setups used with each signaling type.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f			700	MHz	Differential clock outputs, LVDS, LVPECL, FlexSwing
	f			350	MHz	Differential clock outputs, HCSL, LPHCSL
	f			220	MHz	Single-ended (LVCMOS) clock outputs
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature -40°C to 105°C, rated power supply voltage, load variation of 2 pF ±10%, and 10 years aging at 85°C
		–	–	±50	ppm	
Temperature Range						
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage		1.71	1.80	1.89	V	
		2.25	2.50	2.75	V	
		2.97	3.30	3.63	V	
Core Current						
Core Current	Idd	–	49	58	mA	Total current consumed on the VDD and VDDA power domains
GPIO Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Logic High function for all input pins
Input Voltage Low	VIL	–	–	30%	Vdd	Logic High function for all input pins
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -300 µA for GPIO 1, 4, 8, 9 IOH = -300 µA for GPIO 3, 5 IOH = -300 µA for GPIO 2
Output Voltage Low	VOL	–	–	10%	Vdd	IOH = 300 µA for GPIO 1, 4, 8, 9 IOH = 300 µA for GPIO 3, 5 IOH = 300 µA for GPIO 2
Output Characteristics						
Duty Cycle	DC	45	–	55	%	See Figure 13 for waveform
Startup, OE and SE Timing						
Startup Time	T_start	–	1.6	2	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time	T_oe	–	–	600+1 clock cycles	ns	For all signaling types. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 19 for waveform
Output Disable Time	T_od	–	–	600+1 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 20 for waveform
Jitter and Phase Noise, measured at f = 156.25 MHz						
0.012-20 Phase Jitter (Legacy)	T_phj	–	150	200	fs	Measured with phase noise analyzer, integrating between 12 kHz and 20 MHz offset frequency. Recommended for SONET OC-48 applications.
0.012-20 Phase Jitter (with 4MHz HPF)	T_phj	–	110	121	fs	Measured with phase noise analyzer, integrating between 12 kHz and 20 MHz offset frequency. Uses 4 MHz high pass and 20 MHz low pass filters, each with 20 dB/dec roll-off. Includes spurs.
Spurious Phase Noise	T_spn	–	-106	–	dBc	12 kHz to 20 MHz offset frequency range
RMS Period Jitter	T_jitt_per	–	0.45	0.55	ps	Measured based on 10K cycle
Peak Cycle-to-cycle Jitter	T_jitt_cc	–	2.7	3.6	ps	Measured based on 1K cycle
Jitter measured at f = 100 MHz						
PCIe RMS Phase Jitter, Gen 7	T_phj_g7	–	11	16	fs	Compare with PCIe Gen7 (128 GT/s) limit of 67 fs rms
PCIe RMS Phase Jitter, Gen 6	T_phj_g6	–	15	22	fs	Compare with PCIe Gen6 (64 GT/s) limit of 100 fs rms
PCIe RMS Phase Jitter, Gen 5	T_phj_g5	–	25	37	fs	Compare with PCIe Gen5 (32 GT/s) limit of 150 fs rms
PCIe RMS Phase Jitter, Gen 4 and Gen 3	T_phj_g3g4	–	63	93	fs	Compare with PCIe Gen4 (16 GT/s) limit of 500 fs rms and Gen 3 (8 GT/s) limit of 1,000 fs rms

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
PCIe RMS Phase Jitter, Gen 2	T_phj_g2	–	197	291	fs	Compare with PCIe Gen2 (5 GT/s) limit of 3,100 fs rms
PCIe RMS Phase Jitter, Gen 1	T_phj_g1	–	2,243	3,319	fs	Compare with PCIe Gen1 (2.5 GT/s) limit of 86,000 fs rms
Synchronization and Timing						
Output Skew	$t_{SK,B}$	–	24	–	ps	
Spread-Spectrum Generation						
Center Spread		-0.125		+0.125	%	
		-0.25		+0.25	%	
		-0.5		+0.5	%	
Down Spread		-0.25		0	%	
		-0.5		0	%	
Modulation Rate		31.05	31.25	31.8	%	
DCO Mode Characteristics						
Frequency Tuning Range	F_{RNG_DCO}	-800		+800	ppm	Tuning via I2C or SPI
Frequency Step Resolution	F_{RES_DCO}		0.023		ppt	Increment/decrement 36-bit register
Frequency Tuning Clipping Resolution	F_{CLP_DCO}		0.763		ppb	

Table 4. Electrical Characteristics – LVPECL | See Figure 2 and Figure 3 for test setups. Current consumption only accounts for VDDO and output driver stage. Measurements are with VDDO = 3.3 V or 2.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	–	25	mA	Excluding load termination current VDDO=3.3 V
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	–	13	mA	Excluding load termination current VDDO=3.3 V, outputs are Hi-Z
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	–	38	mA	Including load termination current as shown in Figure 24 for VDDO=3.3 V ±10% and R3=220 Ohms
		–	–	36	mA	Including load termination current as shown in Figure 24 for VDDO=2.5 V ±10% and R3=220 Ohms
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	–	26	mA	Including load termination current as shown in Figure 24 for VDDO =3.3 V ±10% and R3=220 Ohms. Driver output is held at last clock output levels.
		–	–	24	mA	Including load termination current as shown in Figure 24 for VDDO =2.5 V ±10% and R3=220 Ohms. Driver output is held at last clock output levels.
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	–	53	mA	Including load termination current. VDDO=3.3 V See Figure 25 for termination
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	–	41	mA	Including load termination current. See Figure 25 for termination. Driver output is held at last clock output levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.075	Vdd-0.95	Vdd-0.86	V	See Figure 12 for waveform, VDD 3.3 V and 2.5 V only
Output Low Voltage	VOL	Vdd-1.84	Vdd-1.7	Vdd-1.62	V	See Figure 12 for waveform, VDD 3.3 V and 2.5 V only
Output Differential Voltage Swing	V_Swing	1.4	–	1.8	V	See Figure 13 for waveform
Rise/Fall Time	Tr, Tf	–	210	300	ps	20% to 80%. See Figure 13 for waveform
Differential Asymmetry, peak-peak	V_da	–	–	85	mV	See Figure 15 for waveform
Differential Skew, peak	V_ds	–	±9	±25	ps	See Figure 16 for waveform
Overshoot Voltage, peak	V_ov	–	–	12	%	Measured as percent of V_Swing. See Figure 17 for waveform
Power Supply Noise Immunity (VDDO)						
Power Supply-Induced Jitter Sensitivity	PSJS	–	8.0	–	fs/mV	50 mV peak-peak ripple on VDD from 10 kHz to 20 MHz
		–	2.0	–	fs/mV	50 mV peak-peak ripple on VDD from 10 kHz to 20 MHz Using RC power supply filter as shown in Figure 2

Table 5. Electrical Characteristics – FlexSwing | See Figure 4 and Figure 5 for test setups. Current consumption only accounts for VDDO and output driver stage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	–	25	mA	Excluding load termination current
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	–	14	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	–	35	mA	Including load termination current, for FlexSwing code "ER". See Figure 24 for VDDO =3.3 V ±10% and R3=220 Ohms
		–	–	35	mA	Including load termination current, for FlexSwing code "ER". See Figure 24 for VDDO =2.5 V ±10%, and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	–	23	mA	Including load termination current, for FlexSwing code "ER". See Figure 24 for VDDO =3.3 V ±10% and R3=220 Ohms. Driver output is held at last clock output levels.
		–	–	23	mA	Including load termination current, for FlexSwing code "ER". See Figure 24 for VDDO =2.5 V ±10%, and R3=220 Ohms. Driver output is held at last clock output levels.
Output Characteristics						
Output High Voltage	VOH	VHn -0.25	VHn	VHn +0.25	V	See Figure 12 for waveform; Refer to Table 10 for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn -0.13	VLn	VLn +0.12	V	See Figure 12 for waveform; Refer to Table 10 for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	2*(VHn-VLn) – 0.37	2*(VHn-VLn)	2*(VHn-VLn) + 0.37	V	See Figure 13 for waveform
Rise/Fall Time	Tr, Tf	–	250	300	ps	20% to 80%. See Figure 13 for waveform
Differential Asymmetry, peak-peak	V_da	–	–	100	mV	See Figure 15 for waveform
Differential Skew, peak	V_ds	–	–	±25	ps	See Figure 16 for waveform
Overshoot Voltage, peak	V_ov	–	–	12	%	Measured as percent of V_Swing. See Figure 17 for waveform
Power Supply Noise Immunity (VDDO)						
Power Supply-Induced Jitter Sensitivity	PSJS	–	10.2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "ER"
		–	2.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "ER". Using RC power supply filter as shown in Figure 4

Table 6. Electrical Characteristics – LVDS | See Figure 6 and Figure 7 for test setups. Current consumption only accounts for VDDO and output driver stage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–		29	mA	Excluding load termination current
Current Consumption, Output Disabled without Termination	Idd_od_nt	–		13	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–		33	mA	Including load termination current. See Figure 28 for termination
Current Consumption Output Disabled with Termination	Idd_od_wt	–		17	mA	Including load termination current. See Figure 28 for termination. Driver output is held at last clock output levels.
Output Characteristics						
Differential Output Voltage	VOD	250	360	450	mV	See Figure 14 for waveform
Delta VOD	ΔVOD	–	–	50	mV	See Figure 14 for waveform
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 14 for waveform VDDO = 3.3 V & 2.5 V
		0.8	0.9	1.0		See Figure 14 for waveform VDDO = 1.8 V
Delta VOS	ΔVOS	–	–	50	mV	See Figure 14 for waveform
Rise/Fall Time	Tr, Tf	–	220	300	ps	Measured 20% to 80% using Figure 28 for termination. See Figure 13 for waveform
Differential Asymmetry, peak-peak	V_da	–	–	50	mV	See Figure 15 for waveform
Differential Skew, peak	V_ds	–	–	±50	ps	See Figure 16 for waveform
Overshoot Voltage, peak	V_ov	–	–	10	%	Measured as percent of VOD. See Figure 18 for waveform
Power Supply Noise Immunity (VDDO = 3.3V)						
Power Supply-Induced Jitter Sensitivity	PSJS	–	8.9	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
	PSJS	–	2.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 6

Table 7. Electrical Characteristics – HCSL | See Figure 8 and Figure 9 for test setups. Current consumption only accounts for VDDO and output driver stage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	–	25	mA	Excluding load termination current
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	–	13	mA	Excluding load termination current
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 12 for waveform
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 12 for waveform
Output Differential Voltage Swing	V_Swing	1.1	1.4	1.6	V	See Figure 13 for waveform
Rise/Fall Time	Tr, Tf	–	250	300	ps	Measured 20% to 80%. See Figure 13 for waveform
Differential Asymmetry, peak-peak	V_da	–	–	90	mV	See Figure 15 for waveform
Differential Skew, peak	V_ds	–	±25	±27	ps	See Figure 16 for waveform
Overshoot Voltage, peak	V_ov	–	–	10	%	Measured as percent of V_Swing. See Figure 17 for waveform
Power Supply Noise Immunity (VDDO)						
Power Supply-Induced Jitter Sensitivity	PSJS	–	6.3	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	2.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 8

Table 8. Electrical Characteristics – Low-Power HCSL | See Figure 10 and Figure 11 for test setups. Current consumption only accounts for VDDO and output driver stage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	–	25	mA	Excluding load termination current, VDDO = 3.3 V
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	–	13	mA	Excluding load termination current, VDDO = 3.3 V
Output Characteristics						
Output High Voltage	VOH	–	–	1.1	V	See Figure 12 for waveform
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 12 for waveform
Output Differential Voltage Swing	V_Swing	1.9	2.0	2.15	V	See Figure 13 for waveform
Rise/Fall Time	Tr, Tf	–	250	300	ps	Measured 20% to 80%. See Figure 13 for waveform
Differential Asymmetry, peak-peak	V_da	–	–	130	mV	See Figure 15 for waveform
Differential Skew, peak	V_ds	–	±40	±57	ps	See Figure 16 for waveform
Overshoot Voltage, peak	V_ov	–	–	10	%	Measured as percent of V_Swing. See Figure 17 for waveform
Power Supply Noise Immunity (VDDO)						
Power Supply-Induced Jitter Sensitivity	PSJS	–	7.2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	2.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 10

Table 9. Electrical Characteristics – Low-Voltage CMOS | Current consumption only accounts for VDDO and output driver stage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 20 MHz						
Current Consumption, Output Enabled	Idd_oe	–	–	15.2	mA	VDDO = 3.3 V
Current Consumption, Output Disabled	Idd_od	–	–	12	mA	VDDO = 3.3 V
Output Characteristics (Standard LVCMOS)						
Output High Voltage	VOH	90%	-	-	V	IOH = -4 mA, VDDO=3.3 V
Output Low Voltage	VOL	-	-	10%	V	IOL = 4 mA, VDDO=3.3 V
Rise/Fall Time	Tr, Tf	–	0.4	0.82	ns	Measured 20% to 80% with default settings. SiT91211 has 20 programmable options for rise-time & fall-time.
Duty Cycle		45	–	55	%	Measured in percentage of clock period
Overshoot Voltage, peak	V_ov	–	–	10	%	Measured as percent of difference between VOH and VOL
Output Characteristics (Regulated LVCMOS)						
Output High Voltage Regulated Range	VDDOreg	0.9		VDDO-0.3	V	Regulated VOH can be programmed with up to 20 steps
Output High Voltage	VOH	90%	-	-	VDDOreg	IOH = -4mA, VDDO=3.3V
Output Low Voltage	VOL	-	-	10%	VDDOreg	IOL = 4mA, VDDO=3.3V
Rise/Fall Time	Tr, Tf	–	0.4	0.6	ns	Measured 20% to 80%, output frequency 20 MHz, load = 8 pF. SiT91211 has programmable options for rise-time & fall-time.
Overshoot Voltage, peak	V_ov	–	–	10	%	Measured as percent of difference between VOH and VOL
Power Supply Noise Immunity (VDDO)						
Power Supply-Induced Jitter Sensitivity	PSJS	–	9.4	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz

FlexSwing Configurations

A FlexSwing output driver performs like LVPECL but provides additional flexible and independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDDO or GND pins.

The VOH and VOL range offered depends on VDDO of the driver. Default values are set to Table 10 and can be programmed in NVM in 30 mV steps. For more detailed settings, please **contact SiTime**.

Table 10. FlexSwing Default Swing Settings

Reference Mode	VDDO Setting (V)	VOH Default (V)	VOL Default (V)
VDD	1.8	1.13	0.40
	2.5	1.55	0.58
	3.3	2.30	1.69
GND	1.8	1.15	0.65
	2.5	1.80	1.20
	3.3	2.60	2.00

Test Circuit Diagrams

A 1.5 pF capacitive load is used at each differential output. Because of the additive input capacitance of the active probe used with the oscilloscope, the output characteristics for all signal types are measured with a total of 2 pF capacitive load.

Test Setups for LVPECL Measurements

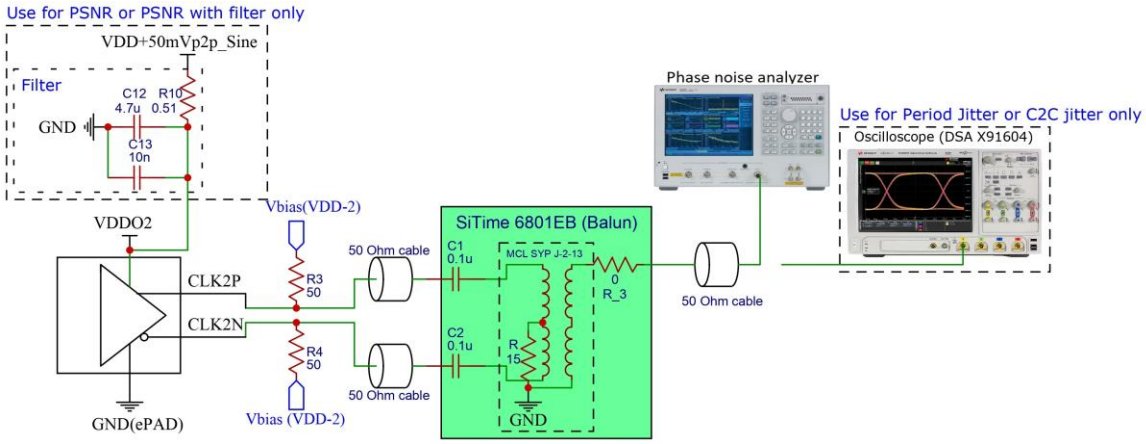


Figure 2. Test setup to measure LVPECL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) without filter added[4]

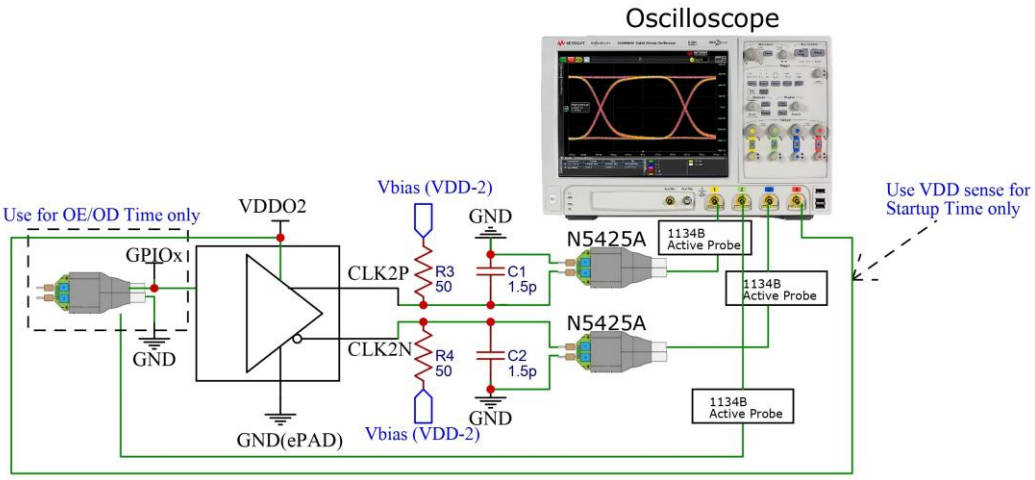


Figure 3. Test setup to measure LVPECL Waveform Characteristics, Current Consumption (with Termination 2)[5], Output Enable/Disable Time, and Startup Time

Notes:

4. See Figure 4 for the test setup to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
5. See Figure 5 for the test setup to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for FlexSwing Measurements[6]

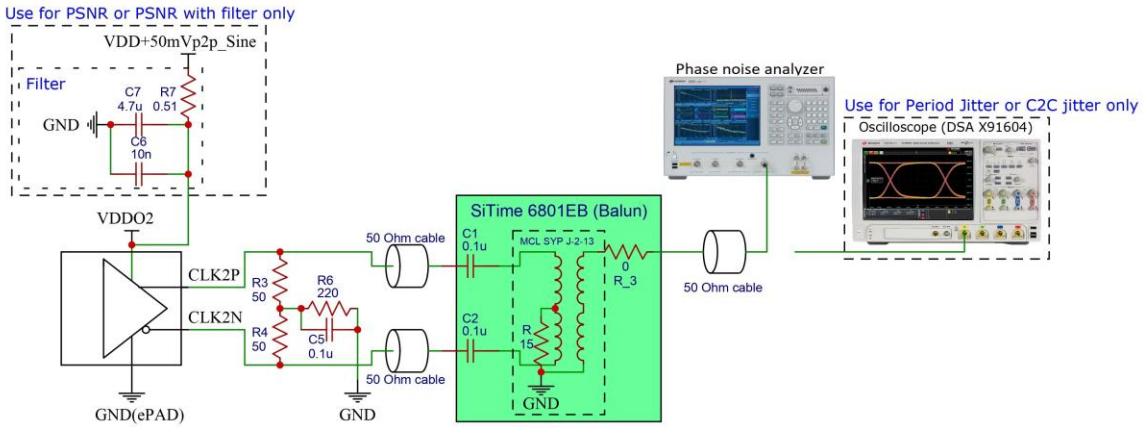


Figure 4. Test setup to measure FlexSwing Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added[7]

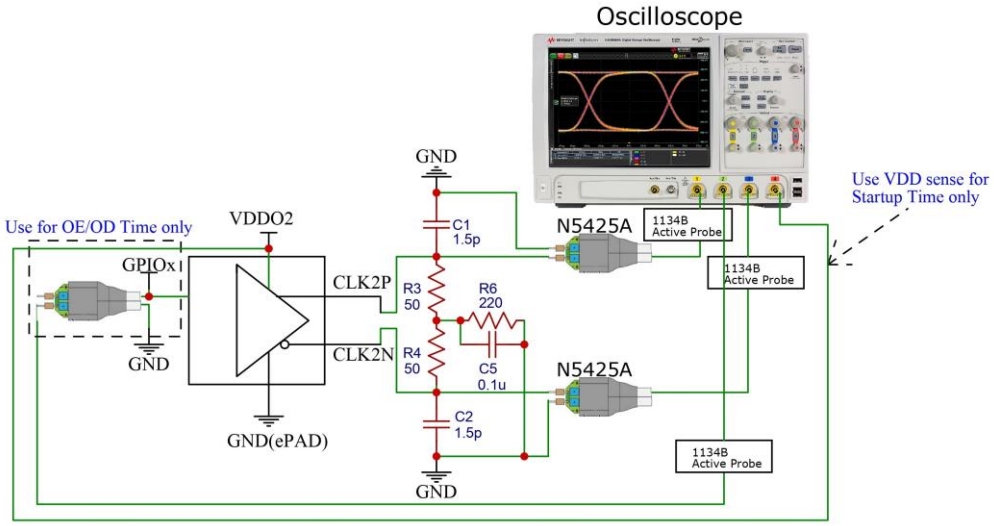


Figure 5. Test setup to measure FlexSwing Waveform Characteristics, Current Consumption[8], Output Enable/Disable Time, and Startup Time

Note:

6. The same test circuits are used for FlexSwing referenced to VDD and FlexSwing referenced to GND.
7. Test setup is also used to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
8. Test setup is also used to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for LVDS Measurements

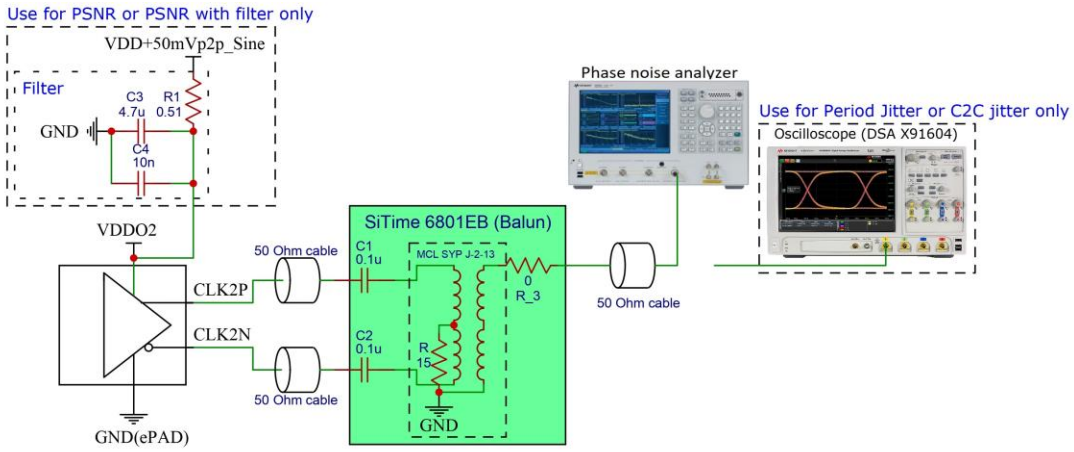


Figure 6. Test setup to measure LVDS Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

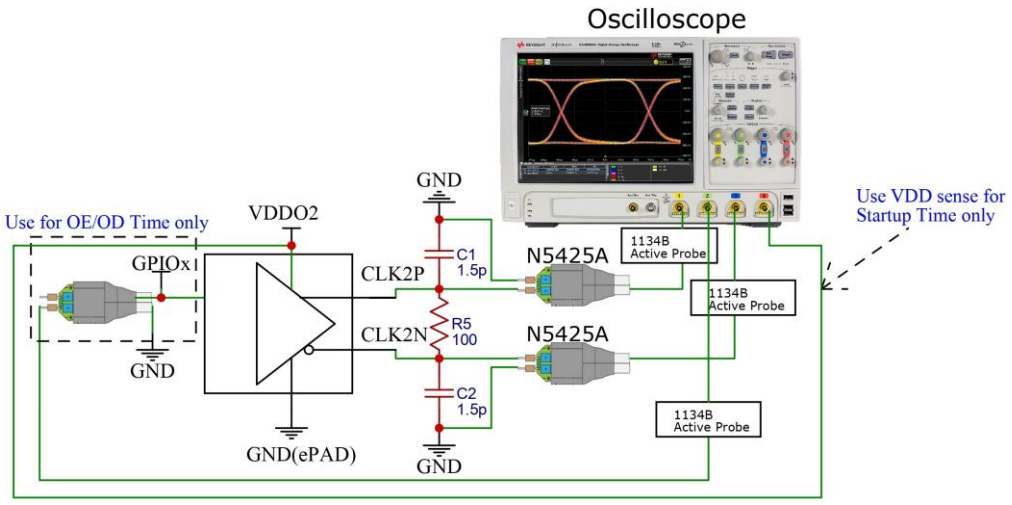


Figure 7. Test setup to measure LVDS Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for HCSL Measurements

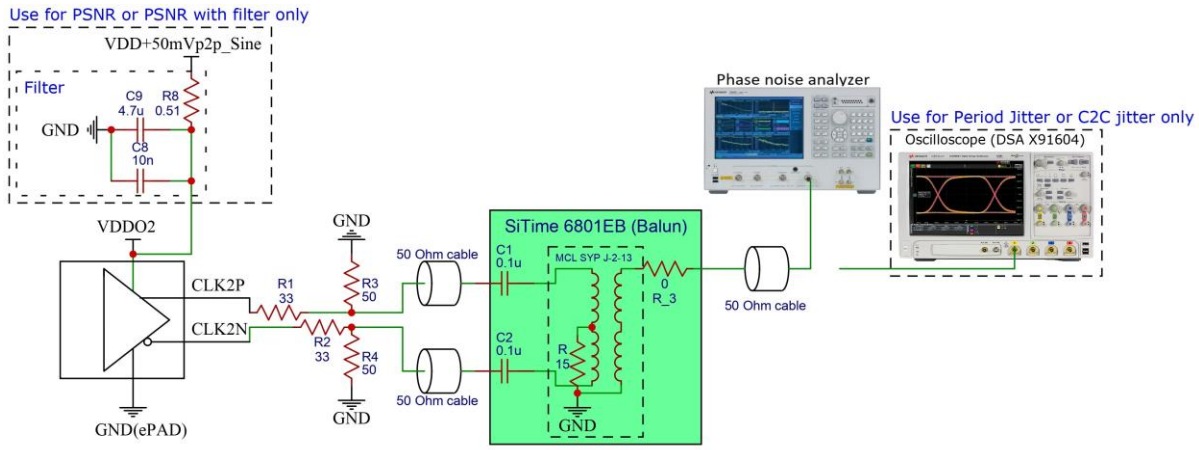


Figure 8. Test setup to measure HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

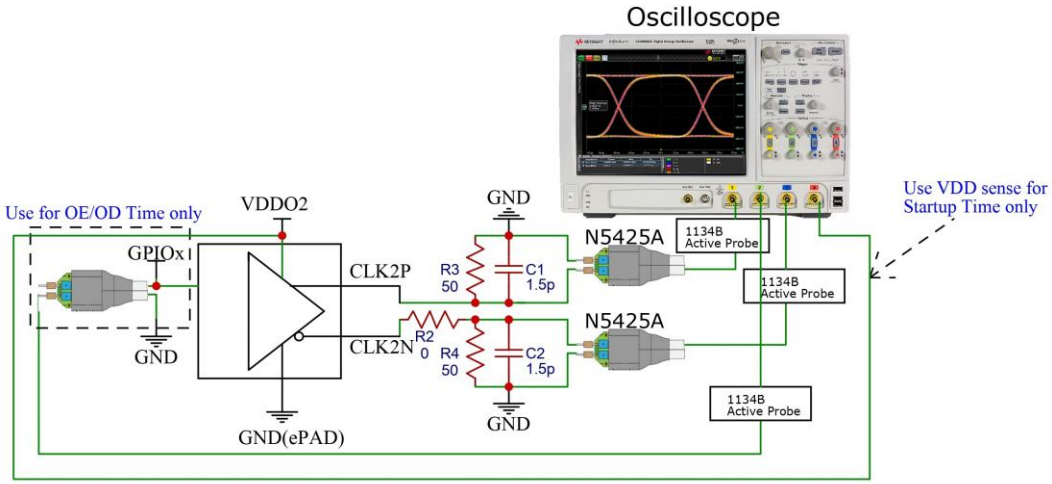


Figure 9. Test setup to measure HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for Low-Power HCSL Measurements

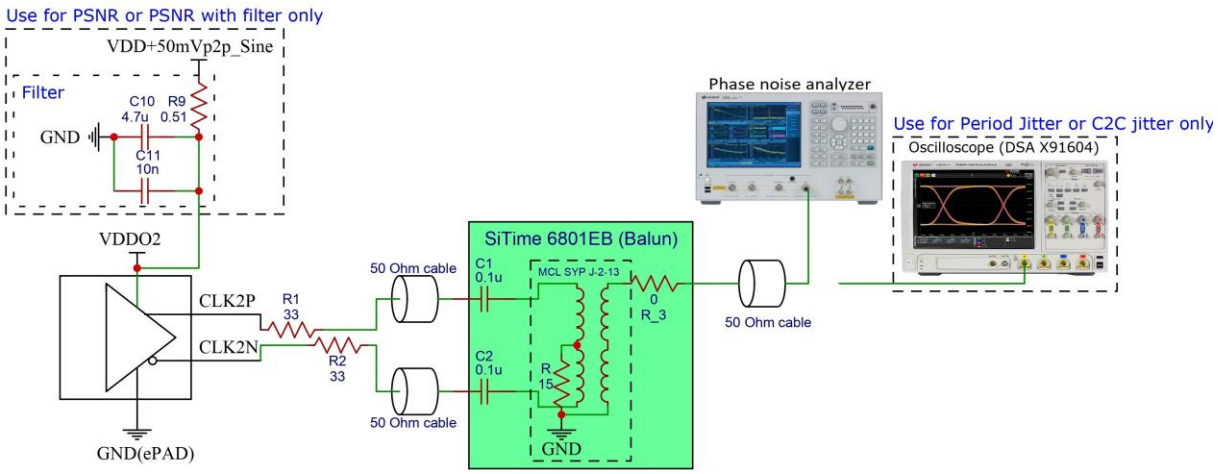


Figure 10. Test setup to measure Low-Power HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

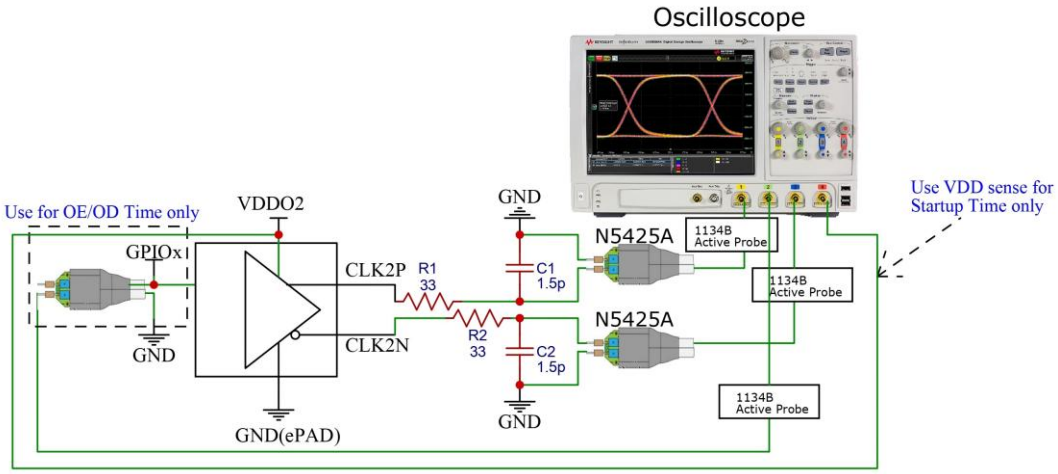


Figure 11. Test setup to measure Low-Power HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Waveform Diagrams

Figure 12. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

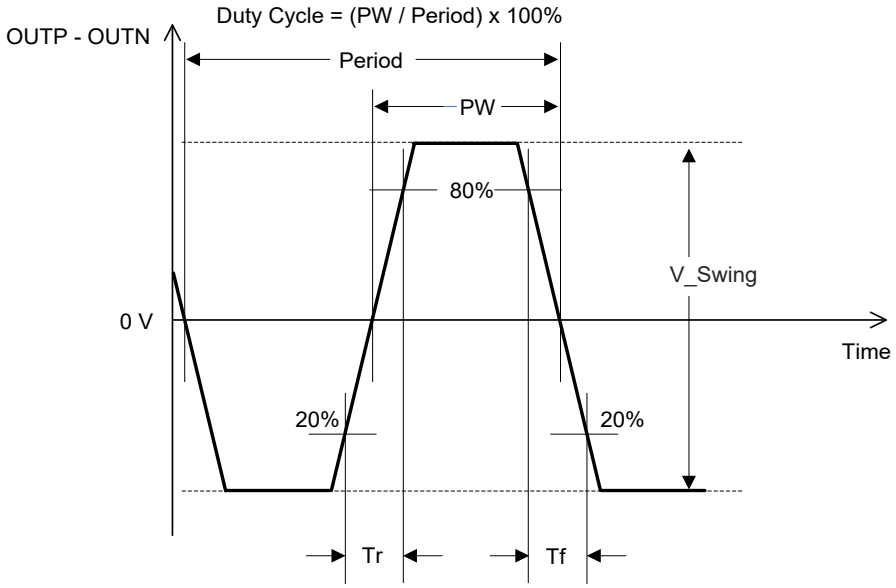


Figure 13. LVPECL, LVDS, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

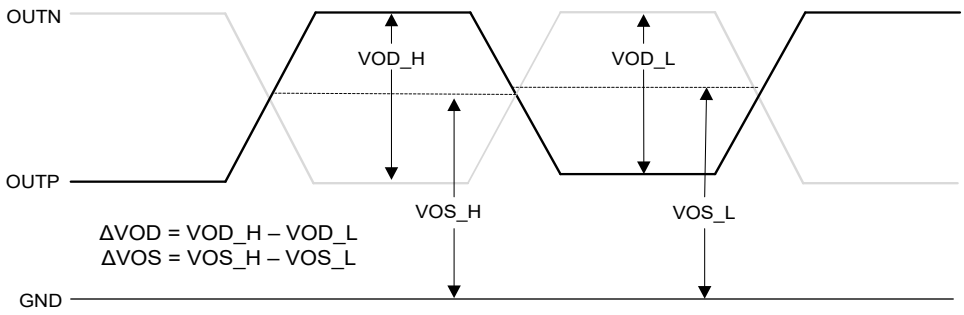


Figure 14. LVDS Voltage Levels per Differential Pin

Waveform Diagrams (continued)

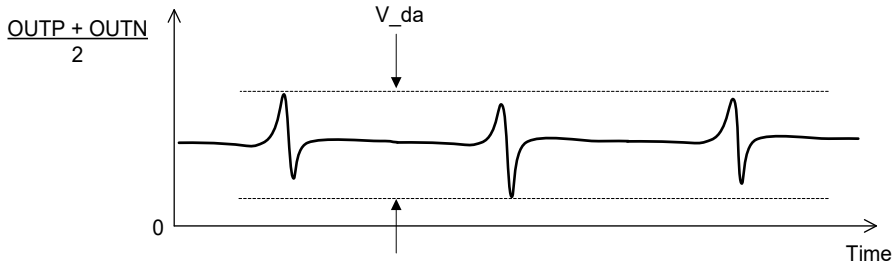


Figure 15. Differential Asymmetry (V_da)

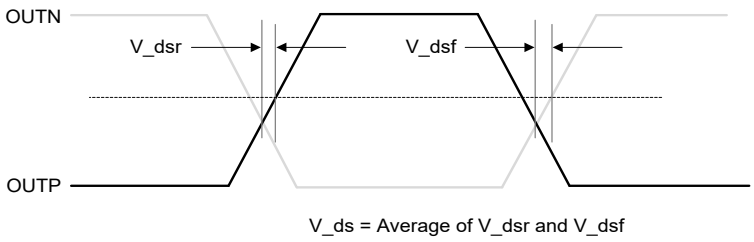


Figure 16. Differential Skew (V_ds) is measured as the Time between the Average Voltage Level and Crossing Voltage

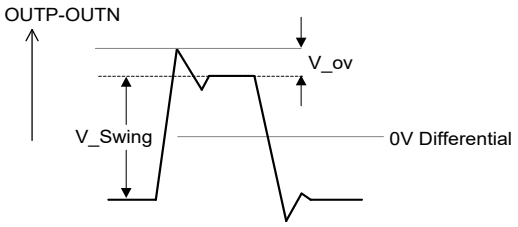


Figure 17. Overshoot Voltage (V_ov) for LVPECL, FlexSwing, HCSL, Low-power HCSL

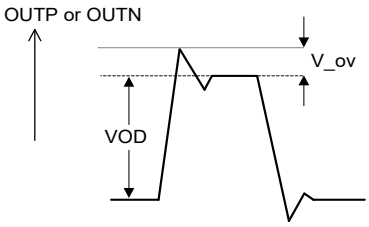


Figure 18. Overshoot Voltage (V_ov) for LVDS Output

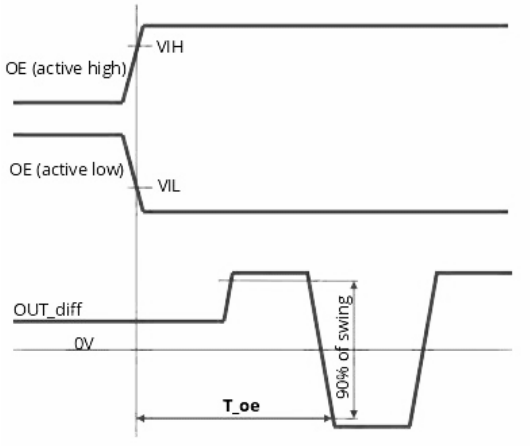


Figure 19. OE Pin Enable Timing (T_oe)

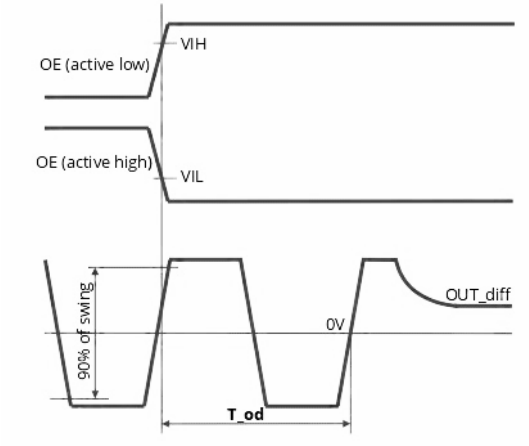


Figure 20. OE Pin Disable Timing (T_od)

Termination Diagrams

LVPECL and FlexSwing Termination

The NeoLite-4 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in Figure 22 and Figure 24, compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_load) into the load termination.

Table 11. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Termination Options					
	Figure 21	Figure 22	Figure 23	Figure 24	Figure 25	Figure 26
LVPECL referenced to Vdd	OK to use I_load = 40 mA with 100 Ω near-end bias resistor	**Do Not Use**	OK to use I_load = 28 mA	OK to use	OK to use I_load = 28 mA	**Do Not Use**
FlexSwing referenced to Vdd	OK to use [9]	OK to use (see Figure 22 for frequency ranges and voltage swings)	OK to use [10]	OK to use	OK to use	**Do Not Use**
FlexSwing referenced to Gnd			**Do Not Use**	OK to use	**Do Not Use**	**Do Not Use**
			Do Not Use	OK to use	**Do Not Use**	OK to use

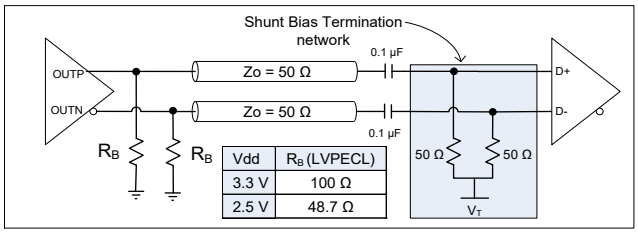


Figure 21. Recommended LVPECL and FlexSwing[9] Termination when AC-coupled

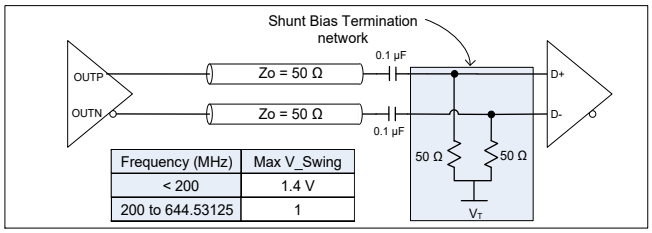


Figure 22. Recommended FlexSwing Termination when AC-coupled

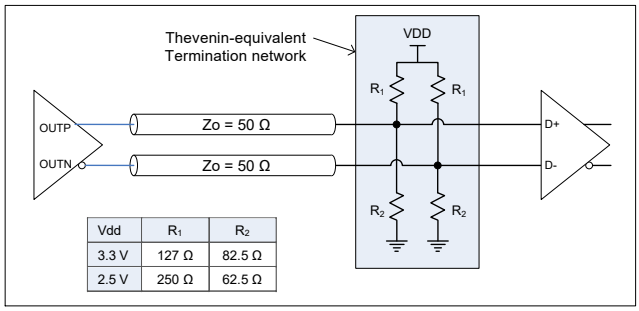


Figure 23. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network[10]

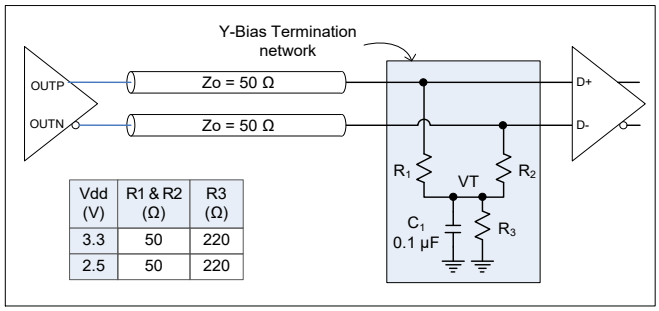


Figure 24. LVPECL and FlexSwing with Y-Bias Termination

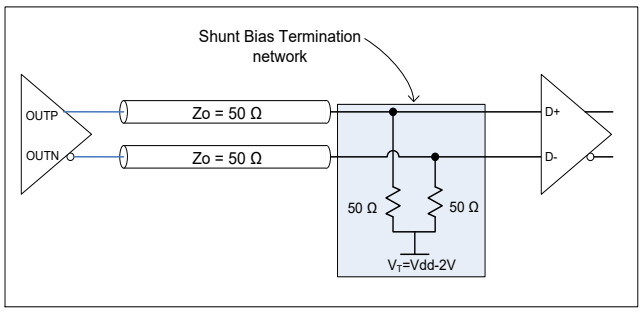


Figure 25. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

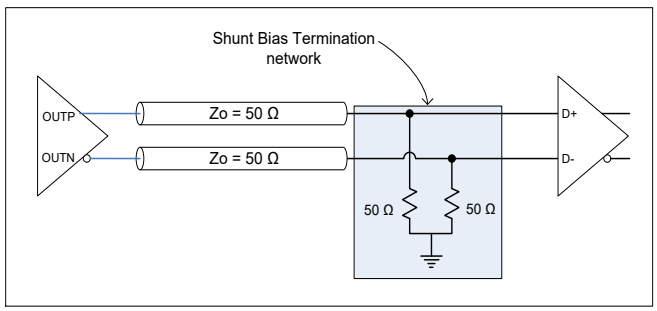


Figure 26. FlexSwing Termination – Only for use with Supply Voltage Order Code "18"

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

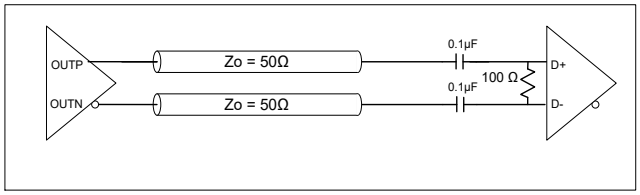


Figure 27. LVDS AC Termination

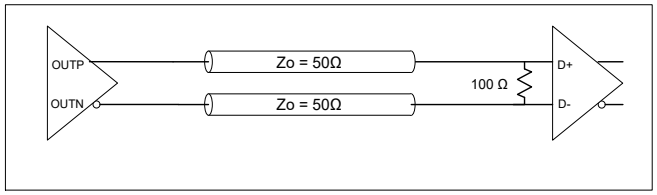
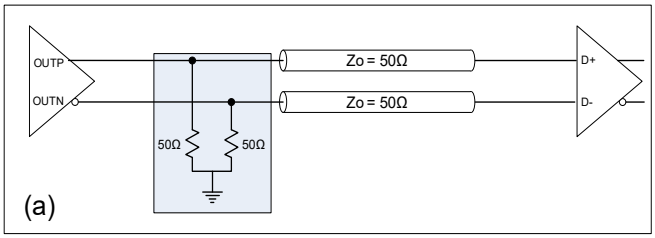


Figure 28. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V



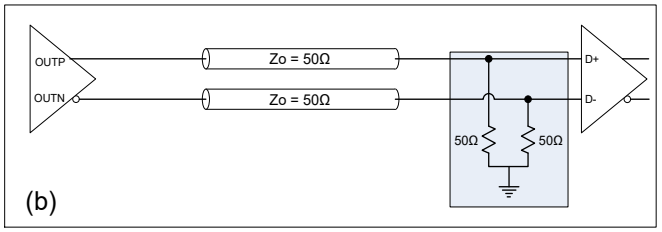


Figure 29. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

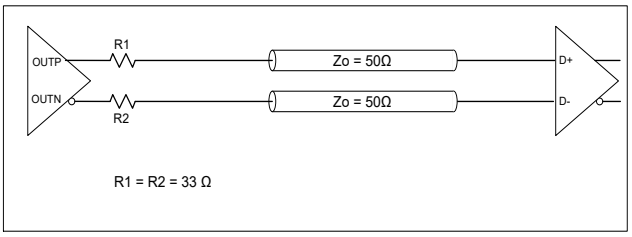


Figure 30. Low-power HCSL Termination

Notes:

9. Contact SiTime for optimum R_B values for FlexSwing options.
10. Contact SiTime for optimum R1 and R2 values for FlexSwing options.

Operating Temperature and Thermal Characteristics

Table 12. Operating Temperature and Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Ambient Temperature	TA	-40		85	°C	Industrial Temperature Range
	TA	-40		105	°C	Extended Industrial Temperature Range
Junction Temperature	TJ			140	°C	
Thermal Resistance Junction to Ambient	θ_{JA}		35		°C/W	Still Air
Thermal Resistance Junction to Case	θ_{JC}		38		°C/W	
Thermal Resistance Junction to Board	θ_{JB}		0.72		°C/W	
Thermal Resistance Junction to Top Center	ψ_{JA}		0.32		°C/W	

Table 13. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
V_{DD}			V
Electrostatic Discharge, HBM 100pF, 1.5kΩ	–	2000	V
Electrostatic Discharge, CDM	-	750	V
Latch up tolerance		JESD78 compliant	
Mechanical Shock Resistance, ΔF/F		10	kG
Mechanical Vibration Resistance, ΔF/F		70	G
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature[11]	–	150	°C

Note:
11. Exceeding this temperature for extended period of time may damage the device.

Table 14. Maximum Operating Junction Temperature[12]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
105°C	140°C

Note:
12. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 15. Environmental Compliance

Parameter	Test Conditions
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL3 @260°C**

Package Pin-Out and Description

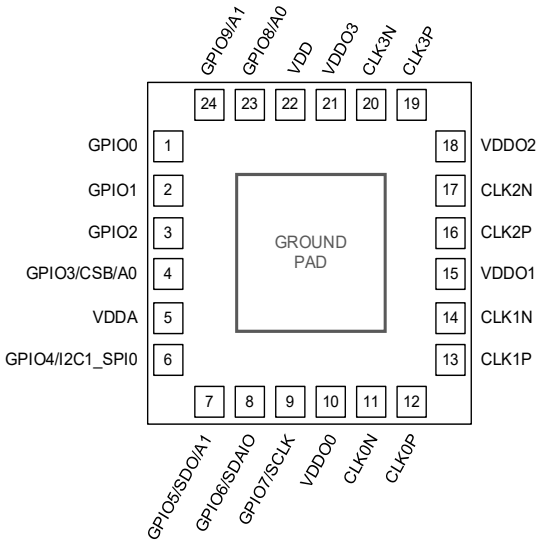


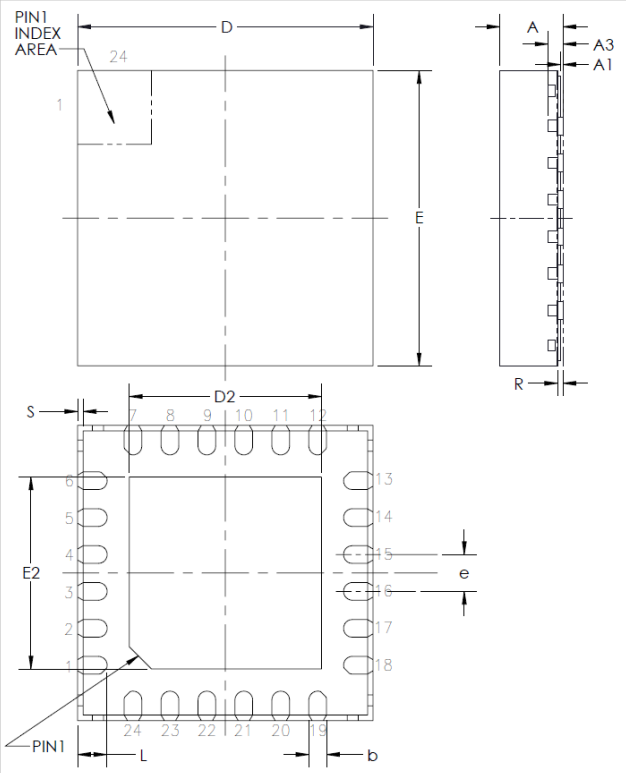
Figure 31. Top View

Table 16. Pin Description

Pin Name	I/O Type	Pin#	Pull-up/Pull-Down	Function
GPIO0	I/O	1	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input
GPIO1	I/O	2	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output
GPIO2	I/O	3	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output
GPIO3/CSB/A0	I/O	4	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output / SPI Chip Select / I2C A0 Address bit
VDDA	PWR	5		Analog Power Supply
GPIO4/I2C1_SPI0	I/O	6	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output / Select between SPI or I2C
GPIO5/SDO/A1	I/O	7	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output / SPI Data Output (SDO) / I2C A1 Address bit
GPIO6/SDAIO	I/O	8		Programmable Input / Output / SPI Input Data (SDI) / I2C Data (SDA)
GPIO7/SCLK	I/O	9		Programmable Input / SPI / I2C Clock
VDDO0	PWR	10		Supply Voltage for CLK0
CLK0N	O	11		Differential / LVCMOS Clock Output
CLK0P	O	12		Differential / LVCMOS Clock Output
CLK1P	O	13		Differential / LVCMOS Clock Output
CLK1N	O	14		Differential / LVCMOS Clock Output
VDDO1	PWR	15		Supply Voltage for CLK1
CLK2P	O	16		Differential / LVCMOS Clock Output
CLK2N	O	17		Differential / LVCMOS Clock Output
VDDO2	PWR	18		Supply Voltage for CLK2
CLK3P	O	19		Differential / LVCMOS Clock Output
CLK3N	O	20		Differential / LVCMOS Clock Output
VDDO3	PWR	21		Supply Voltage for CLK3
VDD	PWR	22		Digital Power Supply
GPIO8/A0	I/O	23	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output / SPI Chip Select / I2C A0 Address bit
GPIO9/A1	I/O	24	Weak Rpu/Rpd=125kΩ/2.5MΩ, NVM select	Programmable Input / Output / SPI Chip Select / I2C A1 Address bit

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

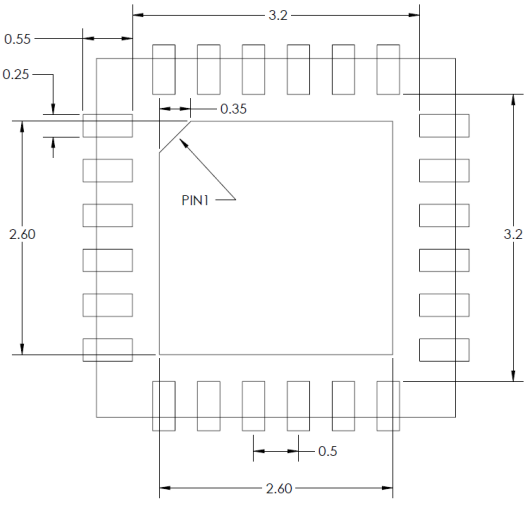


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	0.035	0.05
SUBSTRATE THICKNESS		A3		0.203 ref	
BODY SIZE	X	D		4.00 BSC	
	Y	E		4.00 BSC	
EXPOSED PAD	X	D2	2.50	2.60	2.70
	Y	E2	2.50	2.60	2.70
LEAD PITCH		e		0.50 BSC	
LEAD WIDTH		b	0.19	0.24	0.29
LEAD LENGTH		L	0.30	0.40	0.50
HALF-CUT DEPTH		R	0.075	---	---
HALF-CUT WIDTH		S	---	---	0.075

NOTE
1. ALL DIMENSIONS IN MM

PKG INFO		DRAWING NO.	
24L PQFW 4.00X4.00X0.85 mm		POD-093-PQFW-024-T04040	
		REV	SHEET
DATE	12/05/2023	B02	1 fo 1

Recommended Land Pattern – Dimensions (Unit: mm)



Note: All units in mm.

	PKG INFO	SPL DRAWING NO.	
		SPL-093-PQFW-024-T04040	
DATE	24L PQFW 4.0X4.0 mm	REV	SHEET
12/05/2023		A01	1 of 1

Additional Information

Table 17. Additional Information

Document	Description	Download Link
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption, and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
ECCN #: EAR99	Five-character designation used on the Commerce Control List (CCL) to identify dual use items for export control purposes.	
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	

Revision History

Table 18. Revision History

Version	Release Date	Change Summary
0.0	2-Jun-2022	Initial version
0.1	6-Jun-2022	Spec. updates and Pin out changes
0.2	9-Jun-2022	Additional clean up
0.25	13-Feb-2023	Added Output type specifications Added Dimensions drawings
0.26	28-Feb-2023	Updated Ordering Information with Freq Stability code Organized Additional Information table links
0.28	19-Jul-2023	Updated the Idd current values for all output drivers
0,30	26-Jan-2023	Updated GPIO Table, GPIO inputs configurable active high and low Updated Package Drawings, GPIO tables, pin descriptions
0.31	28-Mar-2024	Updated the PSNR Specs for each output driver
0.40	19-Jun-2025	Updated the DCO function, Power Up Sequence and HCSL source termination
0.98	4-Mar-2026	Updated Parametric Tables, Thermal Characteristics, Functional Description
1.0	1-Sep-2026	Updated disclaimer Final Datasheet

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