SiT7101

10 to 250 MHz, ±0.5 to 5 ppb
Ruggedized MEMS Oven Controlled Oscillator (OCXO)

Description

The Endura® SiT7101 series are the industry's smallest Commercial Off-The-Shelf (COTS) Ruggedized MEMS Oven-Controlled Oscillator (OCXO) (9 mm x 7 mm) to offer over-temp stability as low as ±1 ppb, ±0.01 ppb/°C frequency slope (ΔF/ΔT), and up to 12 hours of holdover time. It features ±0.5 ppb to ±5 ppb stability over a temperature range as wide as -40°C to 95°C. Leveraging SiTime's unique temperature sensing technology and advanced CMOS design, it delivers excellent stability in the presence of environmental stressors – airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The unique modular construction of SiT7101 enables an unmatched combination of class leading stability over temperature, phase noise, programmability, and temperature range all in a compact package. SiT7101 are designed for the best environmental resilience, delivering a precise time reference in the presence of airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The SiT7101 environmental robustness enables unmatched ease-of-use and reduces system manufacturing overhead:

- Highly flexible placement on the PCB
- Minimal shielding for thermal isolation

SiT7101 can be factory-programmed to any frequency between 10 MHz and 250 MHz.

Features

- Up to 12 hours of holdover (±1.5 µs)
- ±0.5 ppb to ±5 ppb frequency stability options over temperature
- ±0.01 ppb/°C frequency slope ΔF/ΔT
- Up to 95°C operating temperature range
- 0.01 ppb/*g* *g*-sensitivity
- 420 mW power consumption – steady state
- 4.5E-12 ADEV at 1-100 seconds averaging time
- Superior stability under dynamic airflow and temperature changes
- Any frequency between 10 MHz and 250 MHz
- Digital frequency pulling (DCOCXO) vis I^2C/SPI
  - Up to ±400 ppm pull range
  - Frequency pull resolution 0.05 ppt (5e-14)
- Integrated regulators for on-chip power-supply noise filtering and excellent PSNR

Applications

- Assured Positioning Navigation Timing
- Guidance Systems
- Data communication
- Radars
- Time holdover and IEEE 1588 synchronization

Order samples

9 mm x 7 mm x 3.6 mm Package

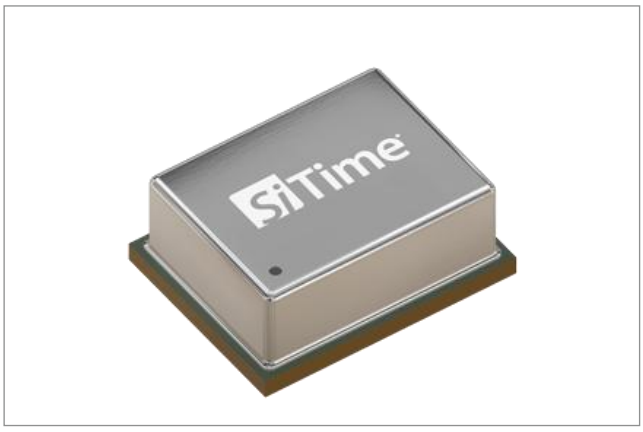


Figure 1. Top and Bottom view

Package Pinout

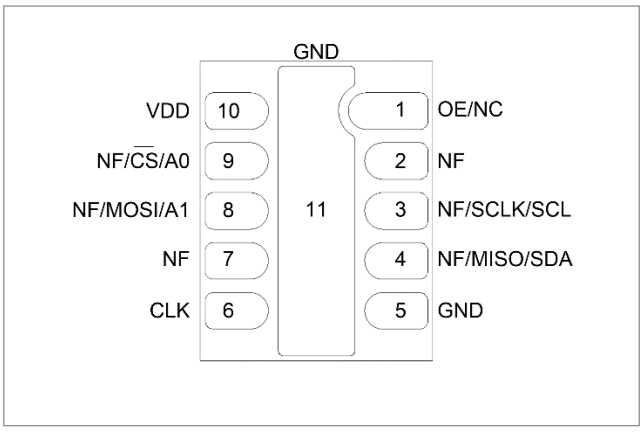
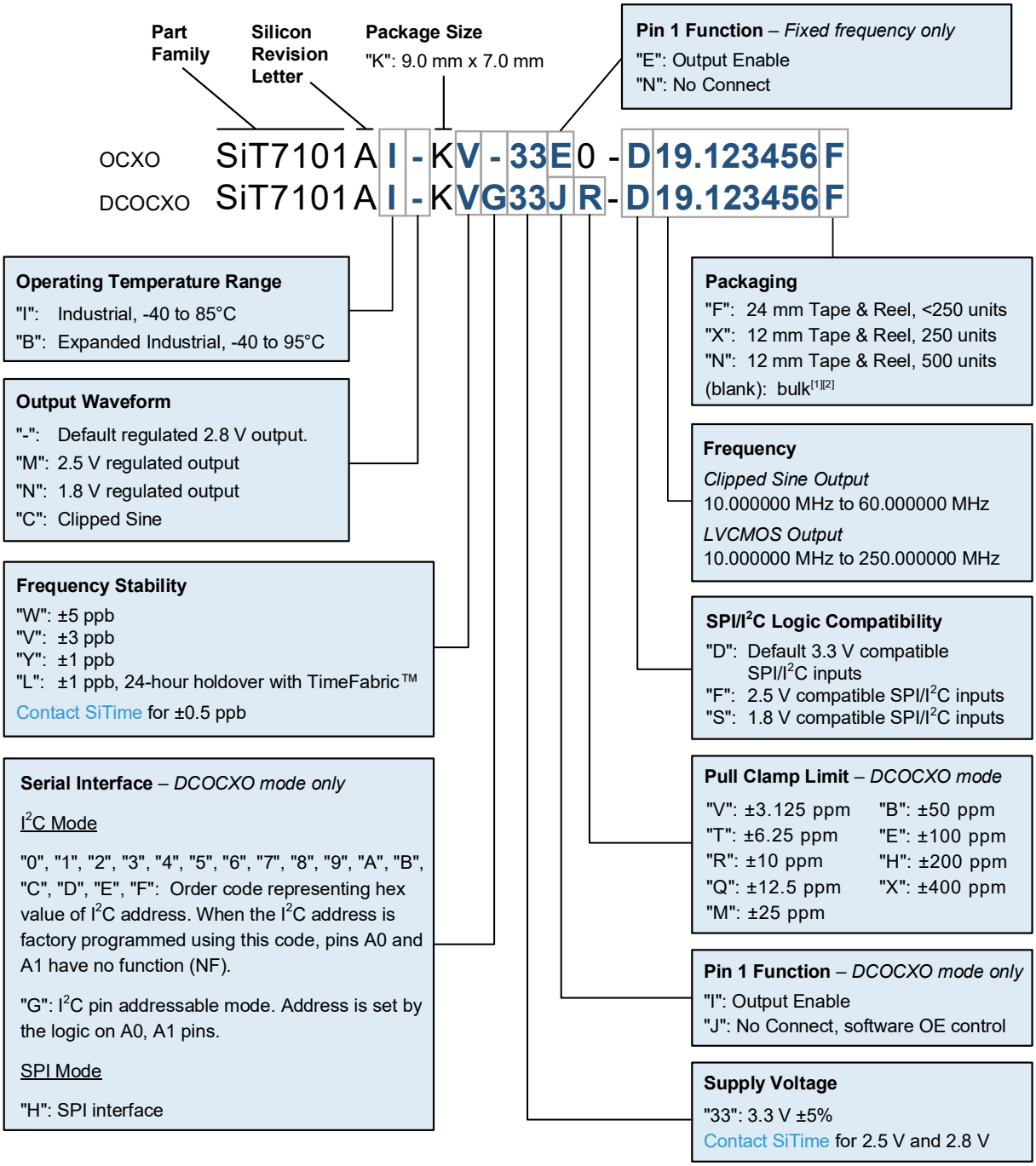


Figure 2. Pin Assignments (Bottom view)

Ordering Information



Notes:

1. Bulk is available for sampling only up to 10 pcs.
2. For quantities of 10 pcs or more, use F for sampling up to 249 pcs for cut-tape.

Table 1. Ordering Codes for Supported Tape & Reel Packaging Method

Device Size	24 mm T&R (<250 units)	24 mm T&R (250 units)	24 mm T&R (500 units)
9 mm x 7 mm	F	X	N

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage. Typical values are at 25°C and 3.3 V VDD. All measurements are specified with 8 pF load unless otherwise stated.

Table 2. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	10	–	250	MHz	LVCMOS Output
		10	–	60	MHz	Clipped Sine Output
Temperature Range						
Operating Temperature Range	T_oper	-40	–	+85	°C	Ambient temperature – option "I"
		-40	–	+95	°C	Ambient temperature – option "B"
Frequency Stability						
Frequency Stability over Temperature	F_stab	–	–	±0.5	ppb	Over operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range. For ±0.5 ppb – Contact SiTime
		–	–	±1		
		–	–	±3		
		–	–	±5		
Acceleration sensitivity (*g*), Gamma Vector	F_g	–	0.01	0.015	ppb/*g*	Low g-sensitivity, total gamma over 3 axes; 15 Hz to 2 kHz; IAW MIL-PRF55310, section 4.8.18.3.1.
Initial Tolerance	F_init	-0.05		0.05	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	-0.03	±0.01	0.03	ppb	±1 ppb. Over operating temperature range (T_oper); Vdd ±5%
		-0.1	±0.04	0.1		±3, 5 ppb. Over operating temperature range (T_oper); Vdd ±5%
Output Load Sensitivity	F_load	-0.003	±0.001	0.003	ppb	±1 ppb. Over operating temperature (T_oper); LVCMOS output, 8 pF ±10%. Clipped sinewave, 10 kΩ || 10 pF ±10%
		-0.010	±0.004	0.010		±3, 5 ppb. Over operating temperature (T_oper); LVCMOS output, 8 pF ±10%. Clipped sinewave, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	ΔF/ΔT	-0.03	±0.01	0.03	ppb/°C	±1 ppb frequency stability over temperature, 1.0°C/min temperature ramp rate, -40 to 95°C
		-0.06	±0.03	0.06		±3 ppb frequency stability over temperature, 1.0°C/min temperature ramp rate, -40 to 95°C
		-0.10	±0.04	0.10		±5 ppb frequency stability over temperature, 1.0°C/min temperature ramp rate, -40 to 95°C
Hysteresis Over Temperature	F_hys	-0.2	±0.1	0.2	ppb	±1 ppb frequency stability over temperature, 1.0°C/min ramp rate, defined as ±ΔF/2
		-0.3	±0.2	0.3		±3 ppb frequency stability over temperature, 1.0°C/min ramp rate, defined as ±ΔF/2
		-0.3	±0.2	0.3		±5 ppb frequency stability over temperature, 1.0°C/min ramp rate, defined as ±ΔF/2
One-Day Aging	F_1d	–	±0.2	–	ppb	±1 ppb At 50°C, after 14-days of continued operation. Aging is measured with respect to day 15
		–	±0.1	–		±1 ppb At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
		–	±0.4	–		±3 ppb and ±5 ppb At 50°C, after 14-days of continued operation. Aging is measured with respect to day 31
		–	±0.3	–		±3 ppb and ±5 ppb At 50°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±30	–	ppb	±0.5 and ±1 ppb . At 50°C, after 2-days of continued operation.
		–	±48	–		±3 ppb and ±5 ppb. At 50°C, after 2-days of continued operation.
20-Year Aging	F_20y	–	±80	–	ppb	±0.5 and ±1 ppb, ±3 ppb and ±5 ppb At 50°C, after 2-days of continued operation.
Total 20-year Stability		–	±130	–	ppb	±0.5 ppb and ±1 ppb
		–	±133	–		±3 ppb
		–	±135	–		±5 ppb

Table 2. Output Characteristics – continued

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Holdover						
4-hour Holdover (mean time error)	H_4h		±0.20		µs	Constant Temperature, 50°C, after 14 days of continuous operation
4-hour Holdover (time error std_dev)	H_4h_std		0.15		µs	Constant Temperature, 50°C, after 14 days of continuous operation
4-hour Holdover (mean time error)	H_4h		±0.10		µs	Variable temperature, after 42 days of continuous operation. See Figure 4
4-hour Holdover (time error std_dev)	H_4h_std		0.20		µs	Variable temperature, after 42 days of continuous operation. See Figure 4
8-hour Holdover (mean time error)	H_8h		±0.85		µs	Constant Temperature, 50°C, after 14 days of continuous operation
8-hour Holdover (time error std_dev)	H_8h_std		0.35		µs	Constant Temperature, 50°C, after 14 days of continuous operation
8-hour Holdover (mean time error)	H_8h		±0.30		µs	Variable temperature, after 42 days of continuous operation. See Figure 4
8-hour Holdover (time error std_dev)	H_8h_std		0.40		µs	Variable temperature, after 42 days of continuous operation. See Figure 4
12-hour Holdover (mean time error)	H_12h		±1.90		µs	Constant Temperature, 50°C, after 14 days of continuous operation
12-hour Holdover (time error std_dev)	H_12h_std		0.6		µs	Constant Temperature, 50°C, after 14 days of continuous operation
12-hour Holdover (mean time error)	H_12h		±0.75		µs	Variable temperature, after 42 days of continuous operation. See Figure 4
12-hour Holdover (time error std_dev)	H_12h_std		0.65		µs	Variable temperature, after 42 days of continuous operation. See Figure 4
Regulated LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	0.6	–	ns	20% - 80% VOH
Output Voltage High	VOH	2.7	2.8	–	V	IOH = +3 mA, "-" default 2.8 V setting
		2.3	2.5	–		IOH = +3 mA, "M" 2.5 V setting
		1.6	1.8	–		IOH = +3 mA, "N" 1.8 V setting
Output Voltage Low	VOL	–	0.05	0.08	V	IOL = -3 mA
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	15%	–	25%	1/F_nom	20% - 80% Vdd
Start-up Characteristics						
Start-up Time	T_start	–	–	10	ms	Time to first pulse, measured from the time Vdd reaches 95% of its final value. Vdd ramp time is 100 µs, 0 V to Vdd
Retrace						
Retrace Accuracy	Retrace		0.10		ppb	24 h ON → 1 h OFF → 1 h ON. Measured according to MIL-PRF-55310F
	Retrace		0.30			24 h ON → 1 h OFF → 24 h ON. Measured according to MIL-PRF-55310F
	Retrace		0.15			24 h ON → 24 h OFF → 1 h ON. Measured according to MIL-PRF-55310F
	Retrace		0.30			24 h ON → 24 h OFF → 24 h ON. Measured according to MIL-PRF-55310F
	Retrace		0.15			24 h ON → 48 h OFF → 1 h ON. Measured according to MIL-PRF-55310F
	Retrace		0.25			24 h ON → 48 h OFF → 24 h ON. Measured according to MIL-PRF-55310F
	Retrace		0.40			24 h ON → 48 h OFF → 48 h ON. Measured according to MIL-PRF-55310F
Time to Frequency Stability	T_stability	–	60	–	s	Time to rated stability over temperature. Device powered on for 48 hours then powered off for 1 hour prior to measurement.
		–	100	–	ms	Time to ±100 ppb frequency stability. Device powered on for 48 hours then powered off for 1 hour prior to measurement.

Table 3. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	VDD	3.14	3.3	3.47	V	Contact SiTime for other voltage options
Supply Voltage Ramp Rate	Vdd_ramp	–	–	0.15	V/µs	
Power Consumption						
Power Consumption – Warm Up	Pwr_warmup	–	750	810	mW	F = 10 MHz, 3.3 V, still air, No load, -40°C
		–	760	830		F = 100 MHz, 3.3 V, still air, No load, -40°C
Power Consumption – Steady State	Pwr_steady	–	420	460		F = 10 MHz, 3.3 V, still air, No load, +60°C
		–	440	480		F = 100 MHz, still air, No load, +60°C

Table 4. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	1000	–	2000	kΩ	Internal pull up to V_{DD}
Input High Voltage	VIH	70	–	–	%	
Input Low Voltage	VIL	–	–	30	%	
Frequency Tuning Range – I²C, DCOCXO mode						
Pull Range	PR	±400	–	–	ppm	DCOCXO mode
Absolute Pull Range[3]	APR	±399.82	–	–	ppm	PR = ±400 ppm
Frequency Pull Clamp Limit[4]	PC_L	±3.125, ±6.25, ±10, ±12.5, ±25, ±50, ±100, ±200, ±400			ppm	DCOCXO mode
I2C Interface Characteristics, 200 Ohm, 550 pF (Max I2C Bus Load), DCOCXO mode						
Bus Speed	F_I2C	≤ 1000			kHz	SDA capacitance <20 pF, 4.7 kΩ aggregate pull-up impedance
		≤ 400				SDA capacitance <50pF, 4.7 kΩ aggregate pull-up impedance
		≤ 100				SDA capacitance <165 pF, 4.7 kΩ aggregate pull-up impedance
Input Voltage Low	VIL_I2C	–	–	30	%	Of regulated I/O voltage
Input Voltage High	VIH_I2C	70	–	–	%	
Output Voltage Low	VOL_I2C	–	–	30	%	
Output Voltage High	VOH_I2C	70	–	–	%	
Input Leakage current	I_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}. Includes typical leakage current from 200 kΩ pull resister to VDD.
Input Capacitance	C_{IN}	–	5	–	pF	
SPI Interface Characteristics, DCTCXO mode						
Bus Speed	F_SPI	≤ 5000			kHz	MISO capacitance <15 pF
		≤ 1000			kHz	MISO capacitance <50 pF
Input Voltage Low	VIL_SPI	–	–	30	%	Of regulated I/O voltage
Input Voltage High	VIH_SPI	70	–	–	%	
Output Voltage Low	VOL_SPI	–	–	30	%	
Output Voltage High	VOH_SPI	70	–	–	%	
Input Capacitance	C_SPI_{IN}		5		pF	
Leakage in High Impedance Mode	I_SPI_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}

Notes:

3. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.
4. Clamp limit is specified at the time of order, which prevents pulling the frequency beyond the specified value.

Table 5. 10 MHz–60 MHz Allan Deviation and Phase Noise – Regulated LVCMOS Output

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Allan Deviation						
$\tau = 1\ second$	AD_1s	–	4.5E-12	–		
$\tau = 10\ seconds$	AD_10s	–	4.5E-12	–		
$\tau = 100\ seconds$	AD_100s	–	4.5E-12	–		
Phase Noise						
1 Hz offset		–	-91	–	dBc/Hz	F = 10 MHz
10 Hz offset		–	-118	–	dBc/Hz	
100 Hz offset		–	-136	–	dBc/Hz	
1 kHz offset		–	-150	–	dBc/Hz	
10 kHz offset		–	-164	–	dBc/Hz	
100 kHz offset		–	-175	–	dBc/Hz	
1 MHz offset		–	-175	–	dBc/Hz	
5 MHz offset		–	-178	–	dBc/Hz	
Jitter						
RMS Phase Jitter (random)	T_phj	–	100	–	fs	F = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
PSNR						
Power Supply-Induced Noise Sensitivity	PSJS		0.04		ps/mV	Power supply ripple from 1 kHz to 10 MHz
Power Supply-Induced Phase Noise	PSPN		-90		dBc	10 MHz output, 50 mVpp noise ripple from 1 kHz to 10 MHz
			-70		dBc	100 MHz output, 50 mVpp noise ripple from 1 kHz to 10 MHz

Table 6. >60 MHz – 250 MHz+ Allan Deviation and Phase Noise – Regulated LVCMOS Output

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Allan Deviation						
$\tau = 1\ second$	AD_1s	–	4.5E-12	–		
$\tau = 10\ seconds$	AD_10s	–	4.5E-12	–		
$\tau = 100\ seconds$	AD_100s	–	4.5E-12	–		
Phase Noise						
1 Hz offset		–	-71	–	dBc/Hz	F = 100 MHz
10 Hz offset		–	-97	–	dBc/Hz	
100 Hz offset		–	-116	–	dBc/Hz	
1 kHz offset		–	-129	–	dBc/Hz	
10 kHz offset		–	-144	–	dBc/Hz	
100 kHz offset		–	-155	–	dBc/Hz	
1 MHz offset		–	-155	–	dBc/Hz	
5 MHz offset		–	-160	–	dBc/Hz	
10MHz offset		–	-167	–	dBc/Hz	
20MHz offset		–	-170	–	dBc/Hz	
Jitter						
RMS Phase Jitter (random)	T_phj	–	100	–	fs	F = 100 MHz, Integration bandwidth = 12 kHz to 20 MHz

Table 7. 10 MHz – 60 MHz Allan Deviation and Phase Noise – Clipped Sinewave Output

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Allan Deviation						
$\tau = 1\ second$	AD_1s	–	4.5E-12	–		
$\tau = 10\ seconds$	AD_10s	–	4.5E-12	–		
$\tau = 100\ seconds$	AD_100s	–	4.5E-12	–		
Phase Noise						
1 Hz offset		–	-91	–	dBc/Hz	F = 10 MHz
10 Hz offset		–	-118	–	dBc/Hz	
100 Hz offset		–	-136	–	dBc/Hz	
1 kHz offset		–	-149	–	dBc/Hz	
10 kHz offset		–	-163	–	dBc/Hz	
100 kHz offset		–	-173	–	dBc/Hz	
1 MHz offset		–	-173	–	dBc/Hz	
5 MHz offset		–	-174	–	dBc/Hz	
PSNR						
Power Supply-Induced Noise Sensitivity	PSJS		0.2		ps/mV	Power supply ripple from 1 kHz to 10 MHz
Power Supply-Induced Phase Noise	PSPN		-68		dBc	60 MHz output, 50 mVpp noise ripple from 1 kHz to 10 MHz

Table 8. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-55 to 105	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[5]		115	°C
Input Voltage, Maximum	Any input pin	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	V

Note:
5. Exceeding this temperature for an extended period of time may damage the device.

Table 9. Thermal Considerations[6]

Package	θ_{JA}[6] (°C/W)	θ_{JB}, Bottom (°C/W)
7.0 mm x 9 mm	Refer to AN10087 Application Note	Refer to AN10087 Application Note

Notes:
6. Measured in still air. Refer to JESD51 for θ_{JA} and θ_{JC} definitions. Devices soldered on a JESD51 2s2p compliant board.

Table 10. Maximum Operating Junction Temperature[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
85°C	**107°C**
95°C	**115°C**

Note:
7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 11. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	20,000	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	30	*g*
Ambient Pressure	**MIL-STD-202 TM 105 Condition C**	70,000	ft
Temperature Cycle	**JESD22, Method A104**	–	–
Solderability	**MIL-STD-883F, Method 2003**	–	–
Moisture Sensitivity Level	**MSL3 @260°C**	–	–

Pin-out Bottom View

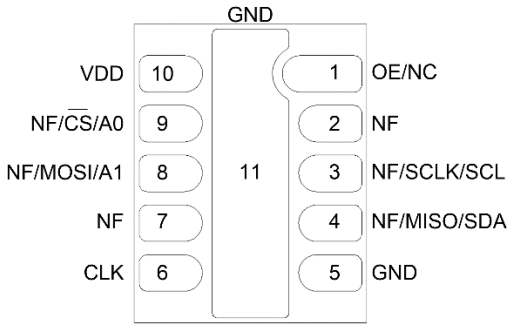


Figure 3. Size 9 mm x 7 mm

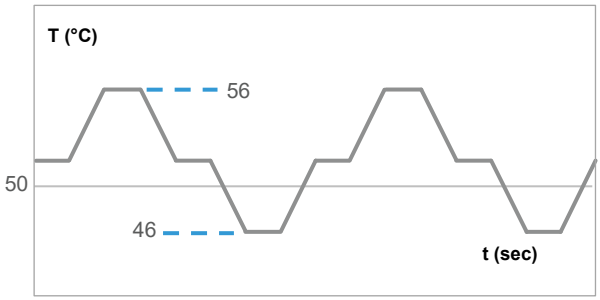
Table 12. Pin Assignments

Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11
OE/NC	NF	NF/SCLK/SCL	NF/MISO/SDA	GND	CLK	NF	NF/MOSI/A1	NF/$\overline{CS}$/A0	VDD	GND

Table 13. Pin Description

Symbol	I/O	Internal Pull-up Resistor	Function
OE	OE – Input	1.2 MΩ Pull-Up	H: specified frequency output L: output is high impedance. Only output driver is disabled. In OE mode, a pull-up resistor of 100 kΩ or less is recommended if Pin 1 is not externally driven. If Pin 1 needs to be left floating, use the NC option.
NC	NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions. Pin 1 voltage should not exceed device VDD or fall lower than device GND. Either of these conditions may lead to frequency shifts larger than specified limits.
NF	NF – No Function	–	Solder to pads. Connect to VDD or leave open If Pin 7 is connected to VDD, a 2 µA leakage current should be expected.
SCLK	SCLK – Input	1.2 MΩ Pull-Up	SPI serial clock
SCL	SCL – Input	1.2 MΩ Pull-Up	I^2C serial clock
MISO	MISO – Output	–	SPI serial data
SDA	SDA – Input/Output	1.2 MΩ Pull Up	I^2C serial data
GND	Ground	–	Connect to ground. Vias from the GND pins to the GND plane should be maximized.
CLK	Output	–	LVCMOS, or clipped sinewave oscillator output
MOSI	MOSI – Input	1.2 MΩ Pull-Up	SPI serial data input
A1	A1 – Input	1.2 MΩ Pull-Up	I^2C address. A0 and A1 decode the I^2C address. See the digital control guide for details. NF when address is specified in the ordering code.
A0	A0 – Input	1.2 MΩ Pull-Up	
$\overline{CS}$	$\overline{CS}$ – SPI Chip Select	1.2 MΩ Pull-Up	SPI Chip select, active low
A0	A0 – Input	1.2 MΩ Pull-Up	I^2C address, least significant bit (LSB), when address is selected via pins
VDD	Power	–	Connect to VDD. Connect 0.01 µF, 1 µF, and 10 µF capacitors in parallel between VDD and GND.

Test Setup and Conditions Diagrams



Char Holdover Profile:

- 20 min soak
- 1°C/min ramp
- 1°C Offset

Figure 4. Variable Temperature – Holdover Temperature Profile

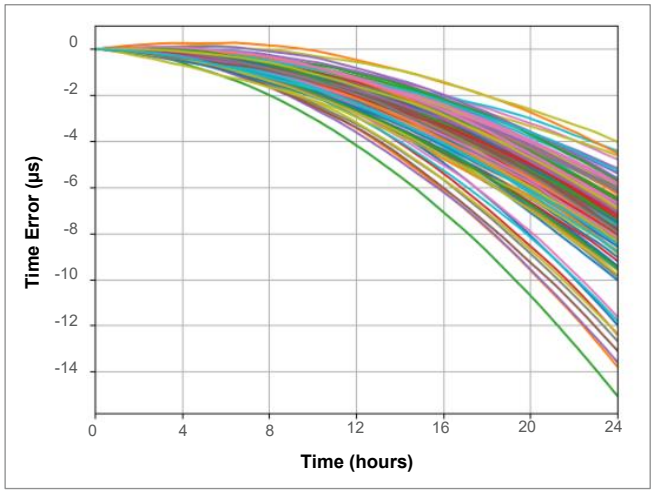


Figure 5. Uncompensated Holdover from 0 to 24 hours
(After 14-days continuous operation, constant temp)

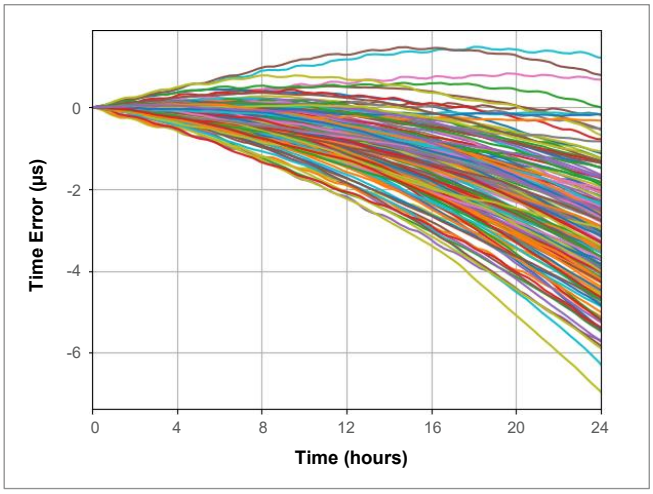


Figure 6. Uncompensated Holdover from 0 to 24 hours
(After 42-days continuous operation, variable temp)

Typical Performance Plots

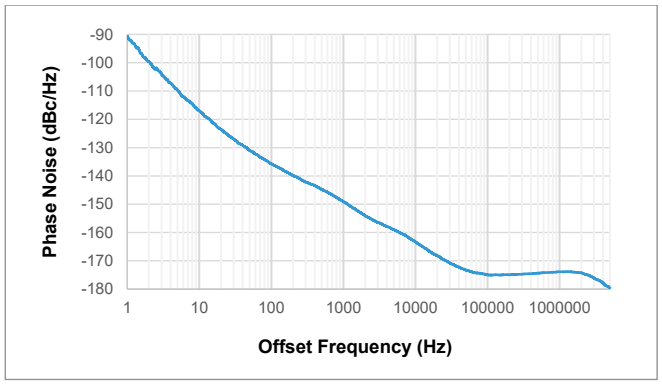


Figure 7. Phase Noise – 10 MHz Fc

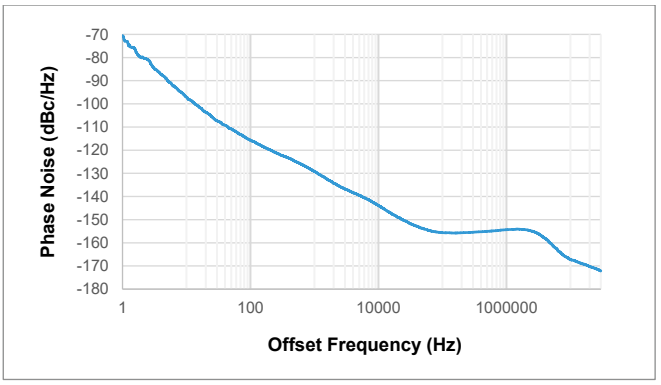


Figure 8. Phase Noise – 100 MHz Fc

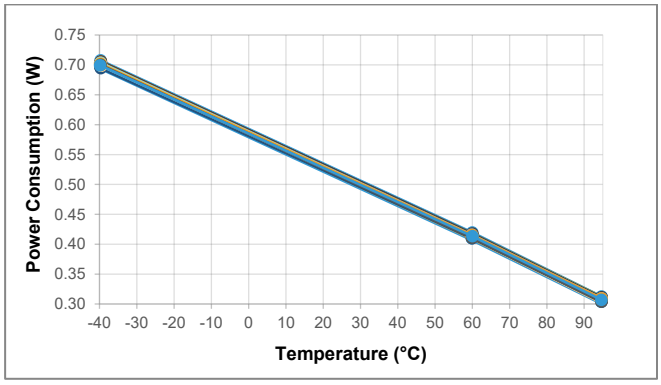


Figure 9. Power Consumption vs Temperature

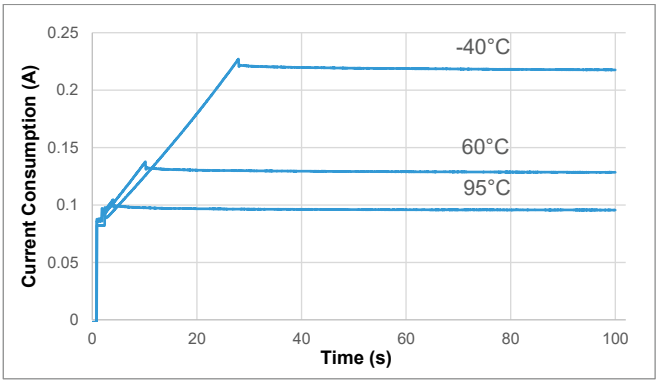


Figure 10. Power-up Ramp Time

Holdover Histograms

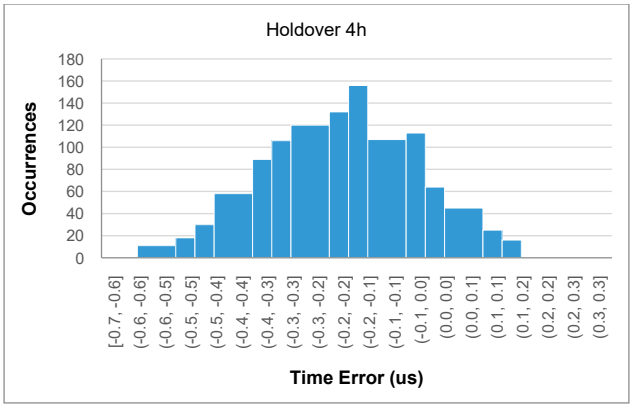


Figure 11. Uncompensated Holdover, 4 hours, Constant Temperature

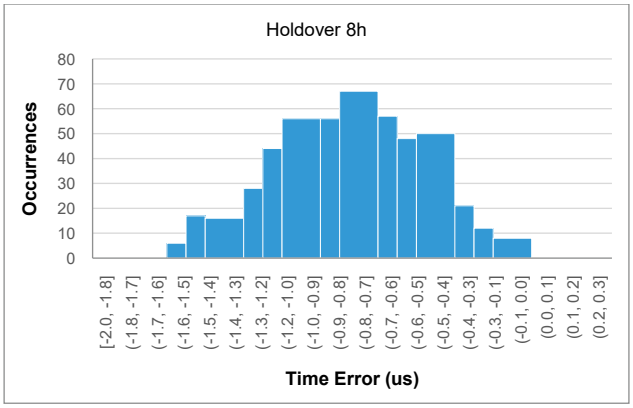


Figure 12. Uncompensated Holdover, 8 hours, Constant Temperature

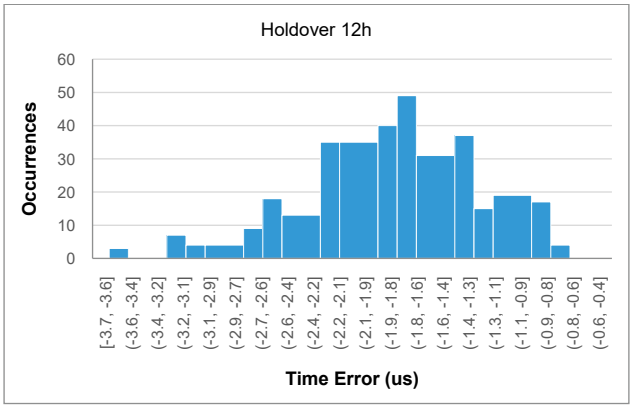


Figure 13. Uncompensated Holdover, 12 hours, Constant Temperature

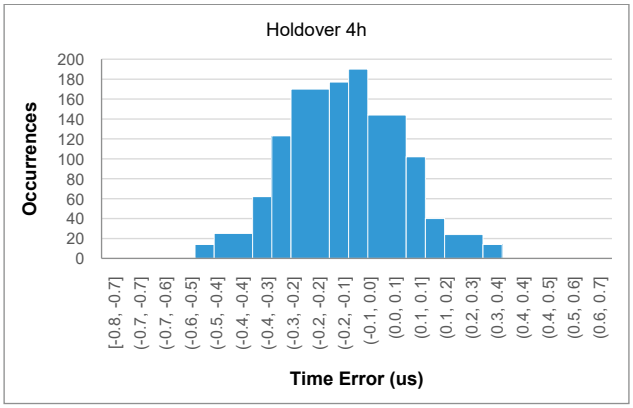


Figure 14. Uncompensated Holdover, 4 hours, Variable Temperature

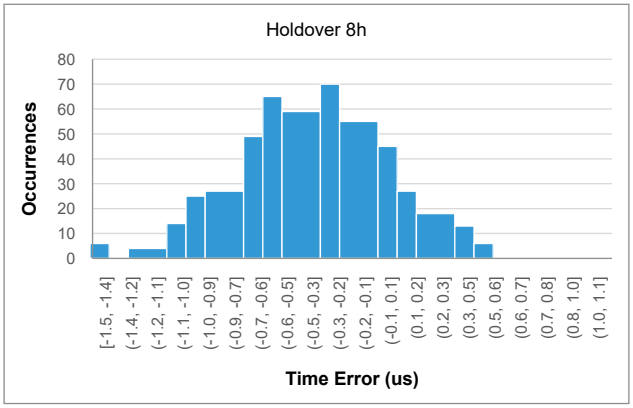


Figure 15. Uncompensated Holdover, 8 hours, Variable Temperature

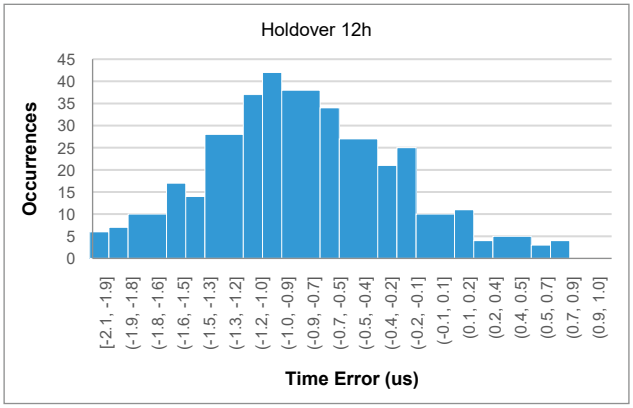


Figure 16. Uncompensated Holdover, 12 hours, Variable Temperature

Board Design Guidelines

Board and Thermal Design Guidelines

For optimal device performance, SiTime recommends adhering to the following board design guidelines. These guidelines ensure that heat generated by SiT7101 is sufficiently expelled through the board.

- The metal layer directly below SiT7101 is a ground plane (e.g., If SiT7101 is seated on M1, M2 is a ground plane).
- The ground plane should be continuous in the 9 x 7 mm x mm area directly under the device.
- Thermal vias are uniformly distributed across the thermal pad. The distance between vias is less than 1.2 mm.
- For a board with more than eight metal layers, at least three are plane layers.
- The metal density in plane layers is maximized.

Contact SiTime for further thermal considerations.

See AN10087 Application Note.

Manufacturing Guidelines

For optimal device performance, SiTime recommends adhering to the following manufacturing guidelines.

- No Ultrasonic or Megasonic Cleaning: Do not subject SiT7101 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- No Reflowing while the SiT7101 is inverted: SiT7101 is a module-based device that must remain upright during reflows.
- Reflow per the JESD22-A113D profile, **not exceeding 2 reflows.**
- After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, it is recommended to use “no clean” flux. Do not subject SiT7101 to liquid based cleaning processes.
- SiT7101 is moisture sensitive and needs to be handled within proper MSL3 guidelines to avoid damage from moisture absorption and exposure to solder reflow temperatures. Deviation from these guidelines may result in yield and reliability degradation.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.
- The SiT7101 package includes a vent hole to allow moisture to escape during the reflow process in compliance with an MSL3 device. High altitude applications are acceptable. If the customer assembly process requires a post reflow cleaning step, please use Isopropyl Alcohol (IPA).
- SiTime recommends the following steps during assembly reflow:
  1) During reflow, do not cover the vent hole.
  2) If there is a post reflow cleaning process, cover the vent hole with Kapton tape or equivalent.
  3) After the cleaning process, remove the Kapton tape vent hole cover.

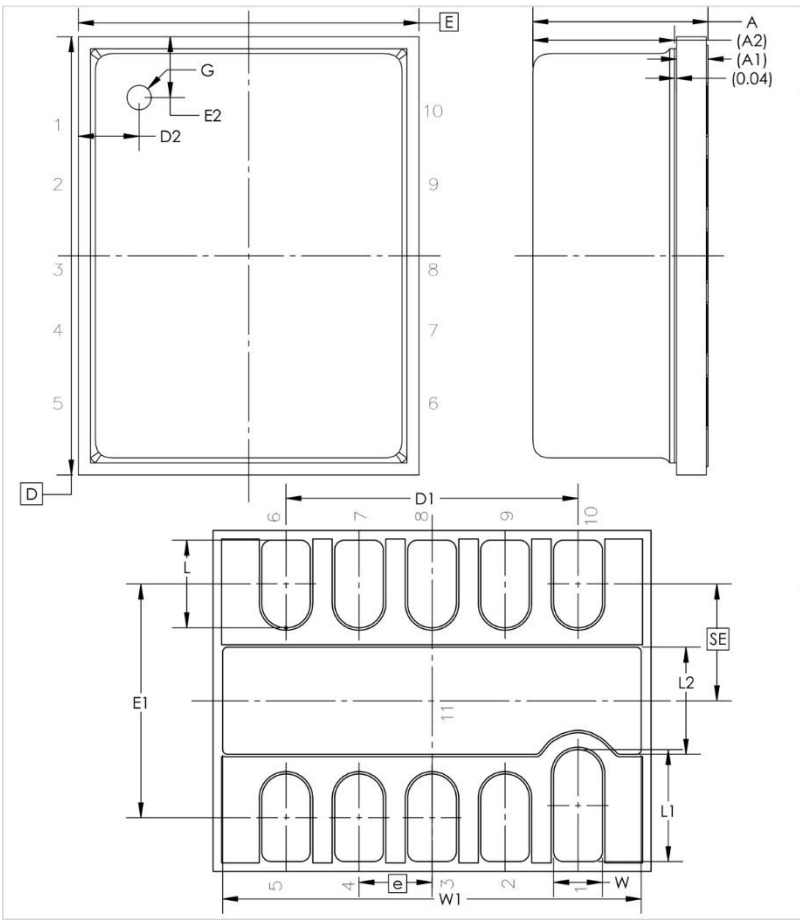
Table 14. Environmental Compliance[8]

Parameter	Condition/Test Method
Moisture Sensitivity Level	**MSL3**
Washability	**Non-Washable**

Notes:
8. This device is RoHS and REACH compliant Pb-free, Halogen-free, and Antimony-free.

Dimensions and Patterns — 9 mm x 7 mm package

Package Size – Dimensions (Unit: mm)



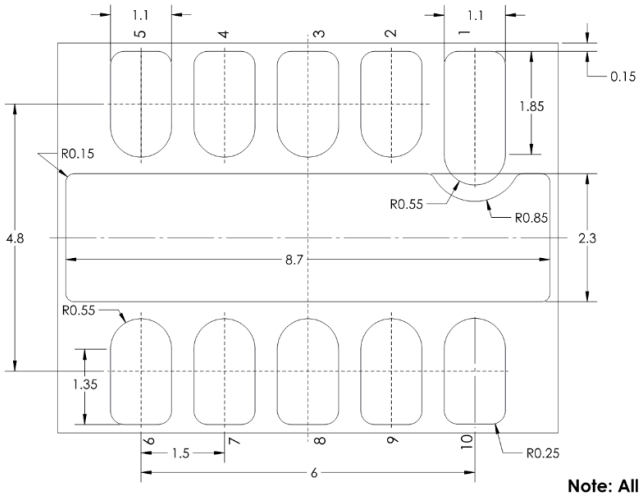
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	3.47	3.60	3.73
SUBSTRATE THICKNESS		A1		0.648 ref	
LID THICKNESS		A2		2.912 ref	
BODY SIZE	X	D		9 BSC	
	Y	E		7 BSC	
LEAD WIDTH		W	0.950	1.000	1.050
		W1	8.550	8.600	8.650
LEAD LENGTH		L	1.750	1.800	1.850
		L1	2.250	2.300	2.350
		L2	2.150	2.200	2.250
LEAD PITCH		e		1.5 BSC	
EDGE LEAD TO LEAD		D1		6.0 BSC	
		E1		4.8 BSC	
BODY CENTER TO CONTACT LEAD		SE		2.4 BSC	
PACKAGE EDGE TOLERANCE		aaa		0.100	
COPLANARITY		ccc		0.080	
Vent Hole Distance		D2		1.250	
		E2		1.250	
Vent Hole Diameter		G		0.500	

NOTE

1. ALL DIMENSIONS IN MM
2. BOTTOM PAD PLATING:
ELECTROLESS Ni: 3-9 µm
ELECTROLESS Pd: 0.02-0.09 µm
IMMERSION Au: 0.025-0.12 µm

PKG INFO	DRAWING NO.	
10L PCBA 9.00X7.00X3.60 mm	POD-089-PCBA-010-C09070	
	REV	SHEET
DATE 11/10/2025	B05	01

Recommended Land Pattern



Note: All units in mm.

PKG INFO	SPL DRAWING NO.	
10L PCBA 9.0X7.0 mm	SPL-089-PCBA-010-C09070	
	REV	SHEET
DATE 05/03/2023	B03	01

Table 15. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6732EBB	https://www.sitime.com/support/resource-library/user-manuals/sit6732ebb-evaluation-board-user-manual-lvcmos

Revision History

Table 16. Revision History

Version	Release Date	Change Summary
0.99	12-Nov-2025	Initial release
1.0	22-Dec-2025	Updated POD drawing; Updated Output Waveform section in the Ordering Information; Updated *g*-sensitivity; Added 0.5 ppb freq stability option; Added Holdover Histograms section

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439